17 999 612 806
MODEL 545 A MICROWAVE FREQUENCY COUNTER
POWER
SAMPLE RATE
GATE
SEARCH
RESET
POWER METER
BAND 1
BAND 2
BAND 3
26 496 310 362
MODEL 548 A MICROWAVE FREQUENCY COUNTER
BAND 4
DISPLAY

Models 545A & 548A
Microwave Frequency Counters

EIP Microwave, Inc.
2731 North First Street, San Jose, CA 95134

TEL: (408) 946-5700
TWX: 910- 338-0155

Manual Part Number: 5580021
Printed in U.S.A., April 1981

545A : CCN 2201
548A : CCN 2301

MANUAL CHANGE INFORMATION
MODEL 545A/548A

At EIP we continually strive to keep up with the latest electronic developments by adding circuit and component improvements to our instruments as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes into the printed manuals immediately. As a result, your counter may contain some or all of the following changes.

PAGE NUMBER	
9-3	Front Card Guide Assembly is now part number 5210199. Rear Card Guide Assembly is now part number 5210200.
08-1	Add to NOTE : When the counter is in REMOTE the RESET key on the front panel keyboard acts as the RETURN TO LOCAL key.
106-3	Q2, Q3, and Q7 are now MMT 3960, part number 4710017. R23 is now 360 ohm, part number 4010361.
108-5	C21 is now part number 2150030. C24 is now part number 2150028. C26 is now part number 2150026. C27 is now part number 2150029.

MANUAL CHANGE INFORMATION

MODELS 545A / 548A

At EIP we continually strive to keep up with the latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested. Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. As a result, your counter may contain some or all of the changes listed below.

IMPORTANT, PLEASE READ

The signatures will change with the revision level of the PROMs that are installed in each counter. Insert this page in your manual as soon as you unpack the instrument. Match your PROMs to the signatures in the following table.

PROM SET, BASIC			
	START	**STOP**	**CLOCK**
CONNECTION	A105 TP14	A105 TP15	A105 TP8
BUTTON	IN	OUT	IN

NODE	**SIGNATURE**								
A105	REV. C	REV.	REV.	REV.	REV.	REV.	REV.	REV.	REV.
JMP 1 pin									
9	**46H8**	**6H1C**							
10	**424H**	**FA74**							
11	**12A5**	**UA55**							
12	**FP59**	**49A0**							
13	**A095**	**1560**							
14	**U155**	**179U**							
15	**A44U**	**40A2**							
16	**1F0H**	**CA4U**							
+5V	**1817**	**1817**							

List of Effective Pages

This List of Effective Pages gives the most recent date on which the technical material on any given page was altered. If a page is simply rearranged due to a technical change on a previous page, it is not listed as a changed page. Within the manual, changes are marked with a vertical bar in the margin.

Pages	Effective Date
FIRST EDITION	*April, 1981*

Printing History

New editions incorporate all update material since the previous edition. The date on the title page changes only when a new edition is published. If minor corrections and updates are incorporated, the manual is reprinted but the date and edition number on the title page do not change.

FIRST EDITION .... April, 1981

Certification

EIP Microwave certifies that this instrument was thoroughly inspected and tested, and found to be in conformance with the specifications noted herein at time of shipment from factory.

Warranty

EIP Microwave warrants this counter to be free from defects in material and workmanship for one year from the date of delivery. Damage due to accident, abuse, or improper signal level, is not covered by the warranty. Removal, defacement, or alteration, of any serial or inspection label, marking, or seal, may void the warranty. EIP Microwave will repair or replace at its option, any components of this counter which prove to be defective during the warranty period, provided the entire counter is returned PREPAID to EIP or an authorized service facility. In-warranty counters will be returned freight prepaid; out-of-warranty units will be returned freight COLLECT. No other warranty other than the above warranty is expressed or implied.

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Section 1
General Information

17 999 6 12 806
MODEL 545A MICROWAVE FREQUENCY COUNTER
26 496 310 362
MODEL 548A MICROWAVE FREQUENCY COUNTER
POWER
SAMPLE RATE
GATE
SEARCH
RESET
POWER METER
BAND 1
BAND 2
BAND 3
BAND 4
REMOTE SENSOR

DESCRIPTION

The 54XA series counters are microprocessor-based heterodyne instruments. The 545A and 548A span the frequency range from 10 Hz to 18 GHz and 10 Hz to 26.5 GHz, respectively. The model 548A, when equipped with frequency extension capability (Option 06), is used in conjunction with a remote sensor (See Model 590) to measure up to 110 GHz.

Using keyboard control, the 54XA series counters provide frequency offsets and frequency selectivity. Options include Power Measurement, full Systems capability via GPIB or BCD/Remote Programming and D/A Converter output.

Full frequency range is covered in three bands. Band 1 is a high impedance input (1 M ohm/20 pF), and spans a 10 Hz to 100 MHz range, with a sensitivity of 25 mV RMS. Band 2 has an input impedance of 50 ohms, a 10 MHz to 1 GHz range, with a sensitivity of −20 dBm. Band 3 has an input impedance of 50 ohms nominal over a range of 1 GHz to 18 (or 26.5) GHz, and a sensitivity to −30 dBm. For frequencies above 26.5 GHz a remote sensor, with an appropriate waveguide input, is called Band 4.

Measurements are presented on a 12 digit LED display that is sectionalized to read GHz, MHz, kHz, and Hz. When the optional power measurement function is activated, the digits on the far right display power in dBm with .1 dB resolution, and frequency resolution is limited to 100 kHz.

SPECIFICATIONS

BAND 1	
RANGE	10 Hz to 100 MHz
SENSITIVITY	25 mV rms
IMPEDANCE	1 MΩ/20 pF
CONNECTOR	BNC (female)
MAX. INPUT LEVEL	120 V rms *
DAMAGE LEVEL	150 V rms *
	* (Above 1 KHz max. input will decrease at 6 dB/octave down to 3.0 V rms.)

BAND 2	
RANGE	10 MHz to 1 GHz
SENSITIVITY	-20 dBm
DYNAMIC RANGE	30 dB
IMPEDANCE	50Ω Nominal
CONNECTOR	BNC (female)
MAX. INPUT LEVEL	+10 dBm
DAMAGE LEVEL	+27 dBm
ACQUISITION TIME	< 50 msec

BAND 3		
RANGE	1 GHz to 18 GHz (26.5 GHz for model 548A)	
SENSITIVITY	-30 dBm: 1 GHz–12.4 GHz -25 dBm : 12.4 GHz– 18 GHz	-20 dBm : 18 GHz–22 GHz -15 dBm : 22 GHz – 26.5 GHz
DYNAMIC RANGE	1 GHz to 12.4 GHz, 37 dB 12.4 GHz to 18 GHz, 32 dB	18 GHz to 22 GHz, 27 dB 22 GHz to 26.5 GHz, 22 dB
IMPEDANCE	50Ω Nominal	
CONNECTOR	Model 545A - Precision type N, (female) Model 548A - APC - 3.5 (female)	
MAX. INPUT LEVEL	+7 dBm	
DAMAGE LEVEL	5 Watts (+37 dBm)	
ACQUISITION TIME	~ 250 msec Independent of frequency	
AUTO AMPLITUDE DISCRIMINATION	(Automatic amplitude discrimination of two frequencies) 10 dB	
FM MODULATION	20 MHz P-P up to 10 MHz rate	
VSWR	< 2.5:1 typical	
FREQUENCY LIMIT	Keyboard control of desired limits (standard). Counter will measure largest signal within programmed limits. Signal outside operating band must be separated by at least 100 MHz from either limit. For signals more than 10 dB above desired signal, separation is typically 200 MHz	

TIME BASE	
FREQUENCY	10 MHz TCXO
AGING RATE	$<|3 \times 10^{-7}|$ per month
SHORT TERM	$<|1 \times 10^{-9}|$ rms for one second averaging time.
TEMPERATURE	$<|2 \times 10^{-6}|$ 0°to + 50°C
LINE VARIATION	$<|1 \times 10^{-7}|$ ± 10% change.
WARM UP TIME	NONE
OUTPUT FREQUENCY	10 MHz, square-wave, 1 V p-p minimum into 50 ohms.
EXT. TIME BASE	Requires 10 MHz, 1 V p-p minimim into 300 ohms.

SPECIFICATIONS, continued

GENERAL	
RESOLUTION	Front panel keyboard input select 1 Hz to 1 GHz
MEASUREMENT TIME	1 msec for 1 KHz resolution 1 sec for 1 Hz resolution
DISPLAY	12 digit LED sectionalized
ACCURACY	± 1 count ± time base error
TEST	Front panel selected diagnostics
SAMPLE RATE	Controls time between measurements variable from 100 msec typ. to 10 sec. Switchable Hold position holds display indefinitely.
RESET	Resets display to zero and initiates new reading
OFFSETS	Keyboard control of frequency offsets (standard) and power offsets (standard with power measurement Option 02). Displayed frequency (power) is offset by entering value to 1 Hz resolution (0.1 dB power).
OPERATION TEMP.	0°C to 50°C
POWER	100/120/220/240/VAC ± 10% (selectable) 50 to 60 Hz, 60 VA typical
WEIGHT, NET	~20 lbs. (9.07 kg)
WEIGHT, SHIPPING	~25 lbs. (11.34 kg)
DIMENTIONS (HWD)	3.5" x 16.75" x 14.0" (89 mm X 425 mm X 356 mm)
ACCESSORIES FURNISHED	Power Cord and Manual

BAND 4

Used with 548A/06 Counter and 590 Frequency Extension Kit

OPTIONS	91	92	93	94
SELECT BAND	41	42	43	44
Waveguide Band	Ka	U	E	W
Range	26.5-40 GHz	40-60 GHz	60-90 GHz	90-110 GHz
Sensitivity (typ)	-25dBm(-20dBm min)	-25 dBm	-25 dBm	-25 dBm
Waveguide Size	Wr-28	WR-19	WR-12	WR-10
Waveguide Flange	UG-599/U	UG-383/U	UG-387/U	UG-387/U
Max. Input (typ)	+5 dBm	+5 dBm	+5 dBm	+5 dBm
Damage Level	+10 dBm	+10 dBm	+ 10 dBm	+10 dBm

EXAMPLE: If desired measurement is 60 — 90 GHz the required equipment is :

Model 548A with Option 06 - Extended Frequency and
Model 590 - Extended Frequency Cable Kit with
Option 93 - Remote Sensor

SPECIFICATIONS, continued

OPTIONS

See Section 10 for detailed information.

01 D TO A CONVERTER
DAC will convert any three consecutively displayed digits into an analog voltage output on rear panel.

02 POWER METER
1 to 18/26.5 GHz will measure sine wave amplitude to 0.1 dBm resolution and display simultaneously with frequency.
Power offset to 0.1 dB resolution, selectable from front panel.
Option will not degrade the basic performance of the counter.

TIME BASE OSCILLATOR OPTIONS:

	03	**04**	**05**
AGING RATE/24 HOURS (After 72 hour warm-up)	$<\|5 \times 10^{-9}\|$	$<\|1 \times 10^{-9}\|$	$<\|5 \times 10^{-10}\|$
SHORT TERM STABILITY (1 second average)	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms
0° to +50° C TEMPERATURE STABILITY	$<\|6 \times 10^{-8}\|$	$<\|3 \times 10^{-8}\|$	$<\|3 \times 10^{-8}\|$
± 10% LINE VOLTAGE CHANGE	$<\|5 \times 10^{-10}\|$	$<\|2 \times 10^{-10}\|$	$<\|2 \times 10^{-10}\|$

06 EXTENDED FREQUENCY CAPABILITY –548A
Use in conjunction with models 590 Frequency Extension kit

07 REMOTE PROGRAMMING/BCD OUTPUT

08 GPIB – Provides programming and output capability per IEEE 488-1978.

09 REAR INPUT

10 CHASSIS SLIDES

Section 2
Installation

INSTALLATION

No special installation intructions are required. The counter is a self-contained bench or rack mounted unit, and only requires connection to a standard, 100/120/220/240V 50-60 Hz power line for operation.

CAUTION

Check current rating of counter fuse and setting of rear panel VAC selector switch before applying power to counter.

COUNTER IDENTIFICATION

This counter is identified by two sets of numbers. The model number 545A or 548A, and a serial number that is located on a label affixed to the rear panel. Both must be mentioned in any correspondence regarding your counter.

SHIPPING AND STORAGE

Wrap the counter in heavy plastic or kraft paper, and repack in original container if available. If the original container can not be used, use a heavy (275 lb test) double-walled carton with approximately four inches of packing material between the counter and the inner carton. Seal carton with strong filament tape or strapping. Mark the carton to indicate that it contains a fragile electronic instrument. Ship to the EIP address on the title page of this manual.

PERFORMANCE CHECKOUT PROCEDURE

The following procedure can be done without special tools or equipment.

1. Turn counter POWER switch off. Check fuse rating and setting of AC POWER switch on the rear panel.
2. Connect the power cord to 100/120 or 220/240 V, 50-60 Hz single-phase power source. The ground terminal on the power cord plug should be grounded.
3. Turn POWER switch on. Dashes will be displayed for about one second, followed by all 0's. This indicates that the automatic self-check has been completed.
4. PRESS: **TEST** ☐ [0] [1] Display should read 200 000 000.
5. PRESS: **TEST** ☐ [0] [2] Display should read all 8's and all annunciators should be lit.
6. PRESS **TEST** ☐ [0] [3] Each display segment should light in turn.
7. PRESS: **TEST** ☐ [0] [4] Each digit should light in turn.
8. This completes the performance checkout procedure.

Section 3
Operation

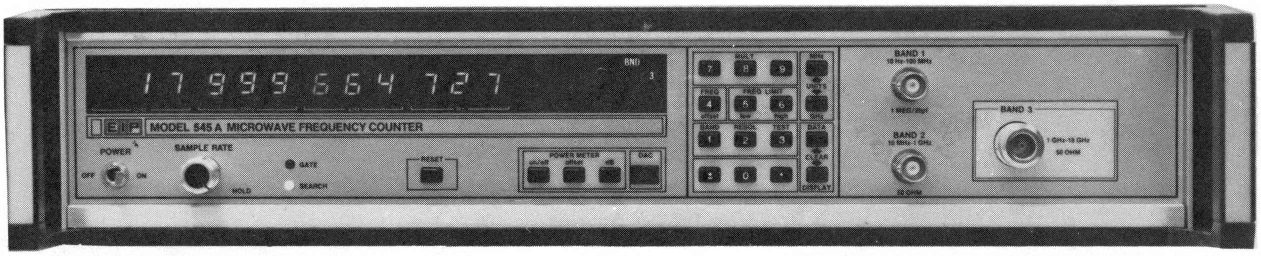

1 7 9 9 9 6 6 4 7 2 7
MODEL 545 A MICROWAVE FREQUENCY COUNTER
POWER
SAMPLE RATE
GATE
SEARCH
RESET
POWER METER
DAC
BAND 1
BAND 2
BAND 3

Figure 3-1. Front Panel, Model 545A

FRONT PANEL CONTROLS AND INDICATORS

DISPLAY

- The 12 digit LED display provides a direct numerical readout of a measurement or of an input frequency. The frequency readout is displayed in a fixed position format that is sectionalized in GHz, MHz, kHz and Hz. Power information is displayed in dBm to 0.1 dB resolution, on the three right-most digits. When both power and frequency are displayed, frequency resolution is limited to 100 kHz.

- POWER switch turns counter on.

- SAMPLE RATE/HOLD varies time between measurements from 0.1 to 10 seconds (nominal). (Gate time is added to sample time, thus the minimum reading for 1 Hz resolution is 1.1 seconds.) The last reading is retained indefinitely in HOLD.

- GATE lights when the signal gate is open and a measurement is being made.

- SEARCH lights when the counter is not locked to an input signal.

- RESET manually over-rides all controls, resets the counter and converter, and initiates a new reading.

OPERATING STATUS

The operating status of the counter is indicated by a series of LEDs. When the counter is displaying input data, instead of a measurement, the appropriate LED status indicator will flash.

- REMOTE lights to indicate that front panel controls are disabled, and that the counter is being controlled by the GPIB option (08), or by the BCD/Remote Programming option (07).
- EXT REF lights to indicate the counter is set to an external time base reference.

CAUTION

When EXT REF lights it does NOT
indicate that correct signal level
has been applied.

- dBm lights to indicate that the Power Meter option (02) is active.
- FRQ LMT, LOW/HIGH lights when frequency limits for Band 3 operation have been selected.
- OFFSET, PWR/FRQ lights when power and/or frequency offsets are stored in the counter memory.
- Band 1, 2, 3, 41, 42, 43, 44 light to indicate which operating range has been selected. When any Band 4 annunciator is lit it indicates that the Extended Frequency Capability option (06) has been selected (Available on 548A only).
- DAC lights to indicate that the Digital-to-Analog Converter option 01 is active.
- MLT lights to indicate the multiplier function is active.

POWER METER/DAC OPTION KEYBOARD

Four keys control the operation of these options.

- ON/OFF push button activates/deactivates power meter .
- OFFSET push button activates the power offset function.
- dB pushbutton acts as a terminator for the input of power offsets.
- DAC pushbutton, followed by two digits (00-12), activates the DAC option. The number keyed in will select the most significant digit (00 = OFF, 01 = 1 Hz, 12 = 10 GHz).

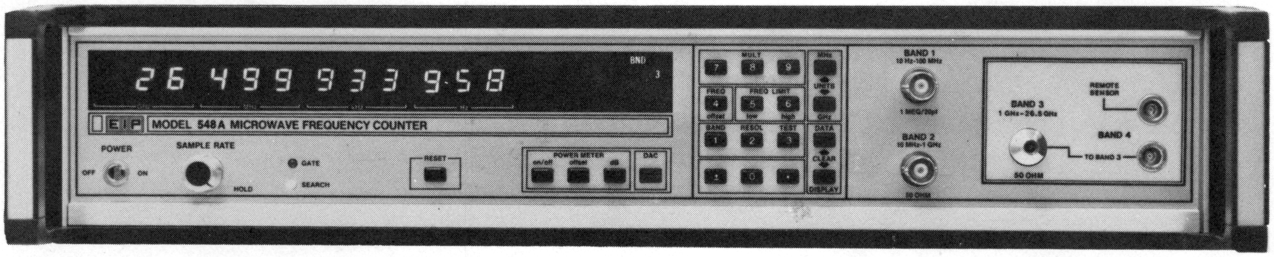

26 499 933 958
BND
3
E I P
MODEL 548A MICROWAVE FREQUENCY COUNTER
POWER
OFF
ON
SAMPLE RATE
HOLD
GATE
SEARCH
RESET
POWER METER
on/off
offset
dB
DAC
MULT
FREQ
offset
FREQ LIMIT
low
high
BAND
RESOL
TEST
MHz
UNITS
GHz
DATA
CLEAR
DISPLAY
BAND 1
10 Hz-100 MHz
1 MEG/20pf
BAND 2
10 MHz-1 GHz
50 OHM
BAND 3
1 GHz-26.5 GHz
50 OHM
REMOTE SENSOR
BAND 4
TO BAND 3

Figure 3-2. Front Panel, 548A

SIGNAL INPUT

- Band 1 input connector (BNC female) has a nominal input impedance of 1 Meg ohms, shunted by 20 pF. It is used for measurements in the range of 10 Hz to 100 MHz.
- Band 2 input connector (BNC female) has a nominal input impedance of 50 ohms. It is used for measurements in the range of 10 MHz to 1 GHz.
- Band 2 input connector on the model 545A is a precision type N female. It is used for counter operation in the range of 1 GHz to 18 GHz. Model 548A has an APC-3.5 female connector that is used for operation in the range of 1 GHz to 26.5 GHz.
- Band 4 is used in conjunction with the Extended Frequency capability option (06), the Model 590 Frequency Extension Cable kit and a remote sensor. Remote sensors are options to the Model 590 and cover waveguide bands from 26.5 to 110 GHz.

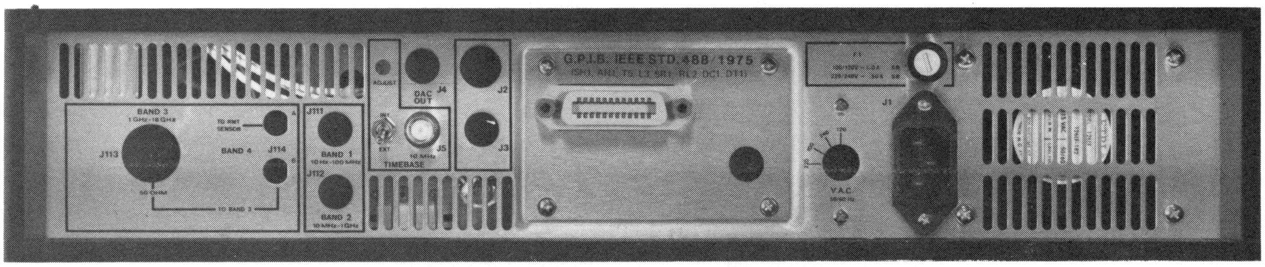

BAND 3
1 GHz - 18 GHz
TO RMT SENSOR
A
J113
BAND 4
J114
B
50 OHM
TO BAND 3
J111
BAND 1
10 Hz - 100 MHz
J112
BAND 2
10 MHz - 1 GHz
ADJUST
DAC OUT
J4
INT
EXT
J5
10 MHz
TIMEBASE
J2
J3
G.P.I.B. IEEE STD. 488/1975
(SH1 AH1 T5 L3 SR1 RL2 DC1 DT1)
F1
J1
120
V.A.C.

Figure 3-3. Rear Panel

REAR PANEL CONTROLS AND CONNECTORS

- AC POWER connector accepts the power cord supplied with the counter.
- FUSE provides overload protection. Use a 1 amp slow-blow MDL type fuse for 100/120 V operation. Use a .50 amp slow-blow FST type fuse for 220/240 V operation.
- VAC SWITCH sets the operating voltage of the counter to match power line. There are 4 settings: 100, 120, 220, and 240 VAC. Counter will operate at voltages within ±10% of selected line voltage, at frequencies of 50 to 60 Hz.

CAUTION

Switch setting and fuse rating must match power line voltage.

- GPIB connector is used with the IEEE 488 - 1978 General Purpose Interface Bus option (08).
- BCD OUTPUT and REMOTE PROGRAMMING connectors (not shown) replace the GPIB connector when the counter is equipped with the BCD OUTPUT/REMOTE PROGRAMMING option (07).
- TIME BASE ADJUST control is used with options 03, 04, or 05 only. Screwdriver adjustment allows precise setting of the internal ovenized crystal oscillator.
- TIME BASE INT/EXT switch selects either the internal time base or an external 10 MHz reference.
- TIME BASE connector (BNC female) allows monitoring of internal 10 MHz time base, or input of an external 10 MHz reference.

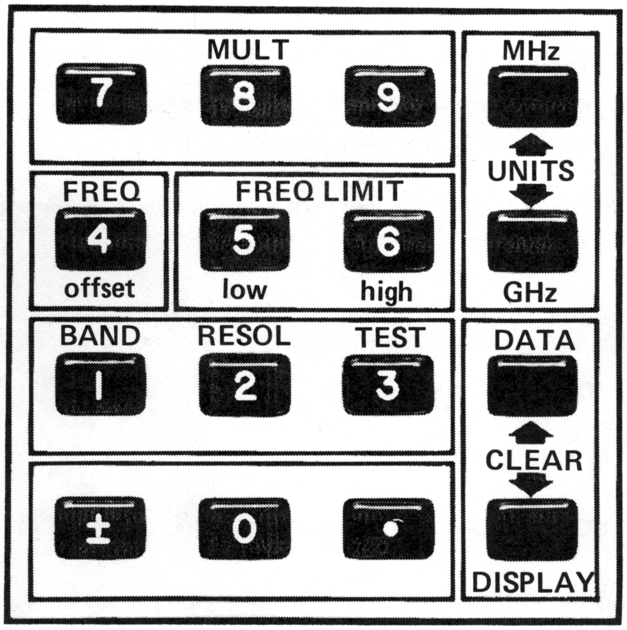


Figure 4-4. Keyboard

KEYBOARD

The keyboard consists of 16 pushbuttons that control major functions of the counter. Twelve keys are used for numerical data entry, the digits 0 through 9, the decimal point and the minus sign. Two keys (MHz and GHz) act as terminators for the input of frequency offset or frequency limits. The CLEAR DATA and CLEAR DISPLAY keys are used to clear stored or displayed data. Seven of the numerical keys are also used to select the band, resolution, test function, frequency offset, frequency limits, and multiplier function.

UNITS (MHz/GHz)

PRESS: MHz ☐ Completes Entry Sequence

PRESS: ☐ GHz Completes Entry Sequence

CLEAR (DATA/DISPLAY)

PRESS: DATA ☐ CLEAR Return "STORED" data of selected function to Power On state. Clears Limits (Low/High), Offsets, DAC, and multiplier operations.

PRESS: CLEAR ☐ DISPLAY Clears display. Does not affect stored data. Restores counter to measurement mode.

BAND SELECTION

To select one of three standard operating bands on the model 545A or 548A.

PRESS: $\overset{\text{BAND}}{\boxed{}}$ $\boxed{1}$ or $\overset{\text{BAND}}{\boxed{}}$ $\boxed{2}$ or $\overset{\text{BAND}}{\boxed{}}$ $\boxed{3}$

Notice annunciator flash and selected band number will light when chosen. This feature allows multiple inputs to be connected and selected in turn.

The "BAND" KEY followed by a numeric key enables the following band selection.

PRESS: $\overset{\text{BAND}}{\boxed{}}$ $\boxed{1}$ 10 Hz - 100 MHz Input

PRESS: $\overset{\text{BAND}}{\boxed{}}$ $\boxed{2}$ 10 MHz - 1 GHz Input

PRESS: $\overset{\text{BAND}}{\boxed{}}$ $\boxed{3}$ 1 GHz - 18 GHz (Model 545A) 26.5 GHz (Model 548A)

On the model 548A equipped with option 06, a 590 cable kit and appropriate optional remote sensor, Band 4 is selected by:

PRESS: $\overset{\text{BAND}}{\boxed{}}$ $\boxed{4}$ $\boxed{X}$

For example, with the 91 Sensor you will press $\overset{\text{BAND}}{\boxed{}}$ $\boxed{4}$ $\boxed{1}$

RESOLUTION / GATE TIME SELECTION

The "RESOL" key followed by a numeric key enables following resolutions.

PRESS:	RESOL	0	1 Hz RESOLUTION
PRESS:	RESOL	1	10 Hz RESOLUTION
PRESS:	RESOL	2	100 Hz RESOLUTION
PRESS:	RESOL	3	1 KHz RESOLUTION
PRESS:	RESOL	4	10 KHz RESOLUTION
PRESS:	RESOL	5	100 KHz RESOLUTION
PRESS:	RESOL	6	1 MHz RESOLUTION
PRESS:	RESOL	7	10 MHz RESOLUTION
PRESS:	RESOL	8	100 MHz RESOLUTION
PRESS:	RESOL	9	1 GHz RESOLUTION

As the resolution is decreased from 1 Hz to 1 kHz, the gate time LED should cycle faster:

- 1 Hz resolution equals a gate time of 1 sec.
- 10 Hz = 100 msec Gate time
- 100 Hz = 10 msec Gate time
- 1 KHz to 1 GHz = 1 msec Gate time

DISPLAY AND DATA ENTRY SEQUENCE

The keyboard display and data entry sequences are segmented into four main groups. All keyboard operations must be started by choosing the function first.

DATA ENTRY - enter offsets or limits

Sequence : 1. FUNCTION , SIGN (plus sign not required) , NUMBER , DECIMAL , NUMBER , UNITS (decimal and second number is optional)

2. FUNCTION , NUMBER

Examples: 1. FREQ OFFSET ± 1 • 2 GHz

2. BAND 2

DISPLAY DATA - display previously entered data

Sequence : FUNCTION , CLEAR DISPLAY

Example : FREQ OFFSET CLEAR DISPLAY

CLEAR DATA - clear entered data

Sequence : 1. FUNCTION , CLEAR DATA

2. FUNCTION , 0 , UNITS

3. FUNCTION , UNITS

Examples: 1. FREQ OFFSET DATA CLEAR

2. FREQ OFFSET 0 GHz

3. FREQ OFFSET GHz

CLEAR ENTRY - clear display before completing data entry

Sequence : FUNCTION , STRING , CLEAR DISPLAY

Example : FREQ OFFSET 1 • 2 CLEAR DISPLAY

MULTIPLY FUNCTION:

In the multiply function the measured frequency is multiplied by an integer up to 99. The result is displayed to 1 KHz resolution. If the results of the multiplications are too big for the front panel to display, the front panel will show F's.

EXAMPLES: PRESS $\overset{\text{MULT}}{\boxed{}}$ AND KEY IN TWO DIGIT NUMBER

EXAMPLE $\overset{\text{MULT}}{\boxed{}}\ \boxed{0}\ \boxed{2}$ FOR MULTIPLIER = 2

NOTE: When "MULT" key is pressed the annunciator "MLT" will flash until the sequence is completed. The two digit multiplier (m) will be displayed as the numbers are entered.

To clear the multiplier function the following operation is performed.

PRESS $\overset{\text{MULT}}{\boxed{}}\ \underset{\text{DATA}}{\overset{\text{CLEAR}}{\boxed{}}}$ or PRESS $\overset{\text{MULT}}{\boxed{}}\ \boxed{0}\ \boxed{1}$

This sequence clears the multiplier function and multiplier (m).

mX ± b

By using the frequency offsets and multiply functions the counter can automatically perform mX ± b calculations.

The equation for the function performed is:

Displayed Reading = mX ± b where m = Multiplier (up to 99) entered from keyboard.

X = Input frequency.

± b = Frequency offset entered from the keyboard.

TO DO mX ± b CALCULATION FOR m = 2, b = -70 MHz

PRESS $\overset{\text{MULT}}{\boxed{}}\ \boxed{0}\ \boxed{2}$ AND $\underset{\text{OFFSET}}{\overset{\text{FREQ}}{\boxed{}}}\ \boxed{\pm}\ \boxed{7}\ \boxed{0}\ \overset{\text{MHz}}{\boxed{}}$

FREQUENCY LIMITS

Frequency limits can be entered to 10 MHz resolution .

PRESS: FREQ LIMIT ☐ low — Notice flashing annunciator.

PRESS: [#] — Number keys corresponding to desired frequency low limit to 10 MHz resolution.

PRESS: MHz ☐ or ☐ GHz — To terminate input sequence. Notice FRQ LMT LOW annunciators solidly lit.

PRESS: FREQ LIMIT ☐ high — Notice flashing annunciator

PRESS: [#] — Key numbers corresponding to desired freq. Hi limit.

PRESS: MHz ☐ or ☐ GHz — To terminate input sequence. Notice FRQ LMT Hi annunciator solidly lit.

To recall stored limits.

PRESS: FREQ LIMIT ☐ low and CLEAR ☐ DISPLAY then FREQ LIMIT ☐ high and CLEAR ☐ DISPLAY

To clear data memory and remove frequency limits.

PRESS: FREQ LIMIT ☐ low and DATA ☐ CLEAR then FREQ LIMIT ☐ high and DATA ☐ CLEAR Vary Source. Notice selected limit(s) are erased. Also notice "FRQ LMT LOW HI" annunciators are out.

NOTE: High and low limits should be separated by at least 100 MHz.

TEST SELECTION

The following tests will verify proper operation of most functional areas of the counter. At the initial turn on the counter performs a RAM and PROM check. During this check dashes are displayed until the check has been completed.

RAM and PROM

The processor writes a sequential bit pattern to each RAM location, then independently reads that pattern. Thus each bit in each location is checked. If the RAM check fails the display will show all "E's". This indicates that the RAM or the RAM decoding is faulty.

The PROM check verifies the PROM bit pattern. If the PROM check fails an error message will be displayed. This indicates that the PROM's or the PROM decoding is faulty. See Section 6.

If both RAM and PROM check are good the counter will begin normal operation about one second after turn on. The counter will now display all 0's.

200 MHz SELF TEST

TEST
PRESS: ☐ 0 1

Notice display is 200 MHz. This verifies operation of the time base reference and it's associated circuits, the signal selection, the count chain, and the local oscillator.

LED TEST

TEST
PRESS: ☐ 0 2

Notice all LED segments and yellow annunciators are lit. This verifies operation of all visual indicators

LED SEGMENT TEST

TEST
PRESS: ☐ 0 3

Notice each segment of each display digit is lit in turn. The sample rate pot will change the rate, and may be adjusted. This checks the segment drivers.

DISPLAY DIGIT TEST

TEST
PRESS: ☐ 0 4

Notice all segments of each digit are lit in turn to verify that each digit operates independently.

The sample rate pot will change the rate, and may be adjusted.

KEYBOARD TEST

PRESS: **TEST** ☐ 0 5

Notice display is 05. Press any key and display will indicate a two digit number showing the position of that key within the matrix thus checking keyboard operations. See table 6-10 for coordinates.

TO EXIT TESTS

PRESS: **CLEAR** ☐ **DISPLAY** to exit a test and return to normal operation.

To exit tests 1 through 4, 6 and 7 you can press any function key. This will exit the test and enter the function selected.

Tests 6 through 10 are used for calibration and troubleshooting. See section 6 and 7.

SET-UP FOR BASIC FREQUENCY MEASUREMENT

Choose the input band by pressing **BAND** ☐ and a number key corresponding to the band. Choose resolution by pressing **RESOL** ☐ and a number key corresponding to required resolution. The signal coupled to the selected input Band Connector will be automatically displayed to the resolution chosen.

NOTE: When pressing the RESOL key the display will go blank for approximately 1/4 second.

FREQUENCY OFFSETS

Frequency OFFSETS can be added or subtracted from the measured value. These OFFSETS can be entered via the front panel keyboard to 1 Hz resolution:

PRESS: **FREQ** ☐ **OFFSET** Notice the flashing annunciator.

PRESS: Number keys corresponding to desired frequency OFFSETS. If OFFSET is to be subtracted press ± and notice polarity sign indicator at far left of display.

PRESS: **MHz** ☐ or ☐ **GHz** to integrate programmed OFFSET into actual frequency measurement. Notice solidly lit annunciator indicating instrument memory is loaded.

PRESS: **FREQ** ☐ **OFFSET** Recalls OFFSET to display, FRQ and OFFSET annunciators flashing.

PRESS: **CLEAR** ☐ **DISPLAY** Notice frequency displayed includes OFFSET; annunciators are lit continuously.

PRESS: **FREQ** ☐ **OFFSET** Recalls OFFSET to display; FRQ and OFFSET annunciators flashing.

PRESS: **CLEAR** ☐ **DATA** Clears data memory and clears offset.
FRQ and OFFSET annunciators are out.
Display is actual frequency without offset.

DISPLAY ERROR MESSAGES

When an error occurs the error number will be displayed. The probable cause of each error is listed below.

OPERATOR ERRORS

The following error messages indicate an operator error.

01 Illegal Key Sequence.

02 A resolution number was not entered.

03 A band number was not entered; or the number entered was too large.

04 No power reading in current band.

05 Frequency limit high > 18.5 GHz, 27 GHz (548A).

06 (Freq Limit HI) – (Freq Limit Lo) < Min. (100 MHz) difference.

07 Frequency Limit Low < .95 GHz (545A/548A).

08

09 Illegal test mode key sequence.

10 Illegal DAC key sequence.

11 Illegal Multiplier key sequence.

12

13 Option not installed.

COUNTER ERRORS

The following error messages indicate a malfunction within the counter.

31	Check sum error	Section 3 PROM	D0000 - DFFF	A105, U13
32	Check sum error	Section 2 PROM	E000 - EFFF	A105, U17
33	Check sum error	Section 1 PROM	E000 - FFFF	A105, U15
34	Check sum error	Power Meter PROM	4000 - 47FF	A107, U20
35	Check sum error	Band 4 PROM	C000 - C7FF	A105, U14
36	Check sum error	GPIB or BCD/Remote PROM	C800 - CFFF	A105, U16

Section 4
Theory of Operation

GENERAL

The 545A and 548A counters automatically measure and display the frequency of an input signal within the range of 10 Hz to 18 GHz for the 545A, and 10 Hz to 26.5 GHz for the 548A. In both models the frequency is divided into three bands.

BAND 1 operates from 10 Hz to 100 MHz. An impedance converter provides an input impedance of 1 M ohm, shunted by 20 pF.

BAND 2 operates from 10 MHz to 1 GHz, using a hetrodyne down converter which converts the input signal into an output signal with a range of 10 MHz to 190 MHz.

BAND 3 operates in the microwave range of 1 to 18 GHz (or 26.5 GHz) and uses a YIG tuned hetrodyne converter to translate the input frequency downward to an intermediate frequency (IF) of 125 MHz.

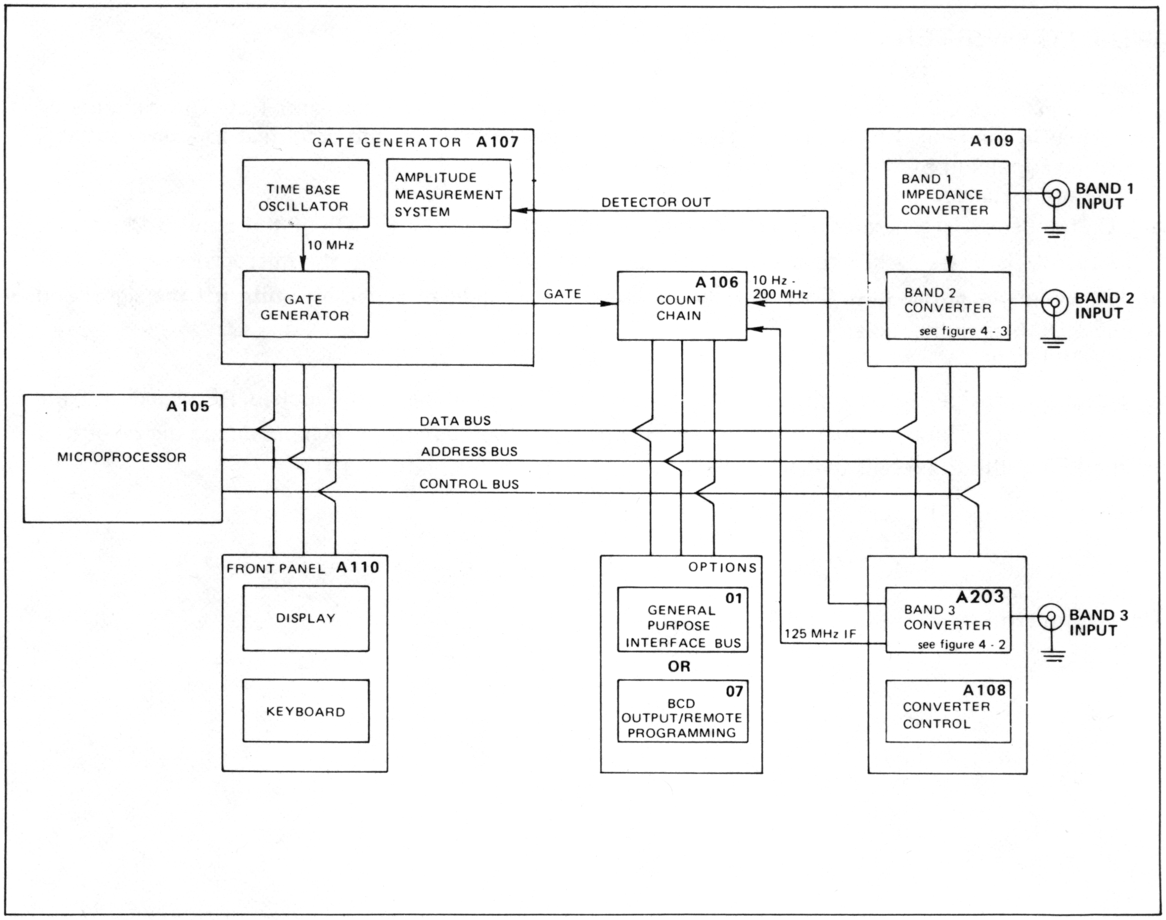

GATE GENERATOR A107
TIME BASE OSCILLATOR
AMPLITUDE MEASUREMENT SYSTEM
10 MHz
GATE GENERATOR
DETECTOR OUT
GATE
A106 COUNT CHAIN
10 Hz - 200 MHz
A109
BAND 1 IMPEDANCE CONVERTER
BAND 1 INPUT
BAND 2 CONVERTER
see figure 4 - 3
BAND 2 INPUT
A105
MICROPROCESSOR
DATA BUS
ADDRESS BUS
CONTROL BUS
FRONT PANEL A110
DISPLAY
KEYBOARD
OPTIONS
01
GENERAL PURPOSE INTERFACE BUS
OR
07
BCD OUTPUT/REMOTE PROGRAMMING
125 MHz IF
A203
BAND 3 CONVERTER
see figure 4 - 2
BAND 3 INPUT
A108
CONVERTER CONTROL

Figure 4-1. Counter Block Diagram, Simplified

BASIC COUNTER

Overall operation is controlled by the Microprocessor Assembly A105. This assembly contains an eight bit microprocessor, its control logic, and the system memory. It communicates with all other assemblies in the instrument by means of a triple bus system: the data, address, and control bus. On each assembly there is a Peripheral Interface Adaptor (PIA) which provides the interface between the bus system and the instrument hardware.

Frequency measurements are performed by comparing an unknown signal to a reference frequency, namely the time base. A 10 MHz crystal oscillator is used as the internal reference and is a part of the Gate Generator Assembly A107. For increased accuracy and stability, ovenized oscillator options are available, or the user may select an external 10 MHz reference.

A frequency measurement is made by generating a time interval (Gate Time) consisting of a number of cycles of the reference. This Gate Time is then used as an interval during which the input signal is counted by the Count Chain Assembly A106.

Initially, the microprocessor selects one of several available inputs to the Count Chain Assembly and the appropriate Gate Time based on user input information; band selection, resolution, etc. The microprocessor then initiates the measurement cycle by resetting the Count Chain to zero and allowing a gate to be generated. During the gate interval, the Count Chain accumulates the number of cycles of the input signal. At the end of the gate time, the microprocessor reads the stored information in the Count Chain and performs any required calculations necessary to convert the measurement into a direct reading of the unknown frequency. The front panel display is then updated with the new measurement results. Figure 4-1 shows a simplified block diagram of the counter.

BAND 2 CONVERTER

An input signal is applied to the mixer along with an appropriate local oscillator (L.O.) to generate an IF frequency in the range of 10 MHz to 190 MHz. This signal is filtered and amplified to a level suitable for direct measurement by the Count Chain.

The L.O. frequency is generated by the Voltage Controlled Oscillator (VCO) of the Band 3 Converter. This frequency is phase locked to the counter's time base and controlled by the microprocessor. A VCO multiplier serves to either pass along the signal directly or double it. It can also turn off the signal and pass only a DC bias to the mixer.

Two detectors provide outputs proportional to the amplitudes of both the applied RF signal and the resulting IF signal. These outputs are compared in the Signal Comparator, which provides a digital output when the IF amplitude exceeds the RF amplitude.

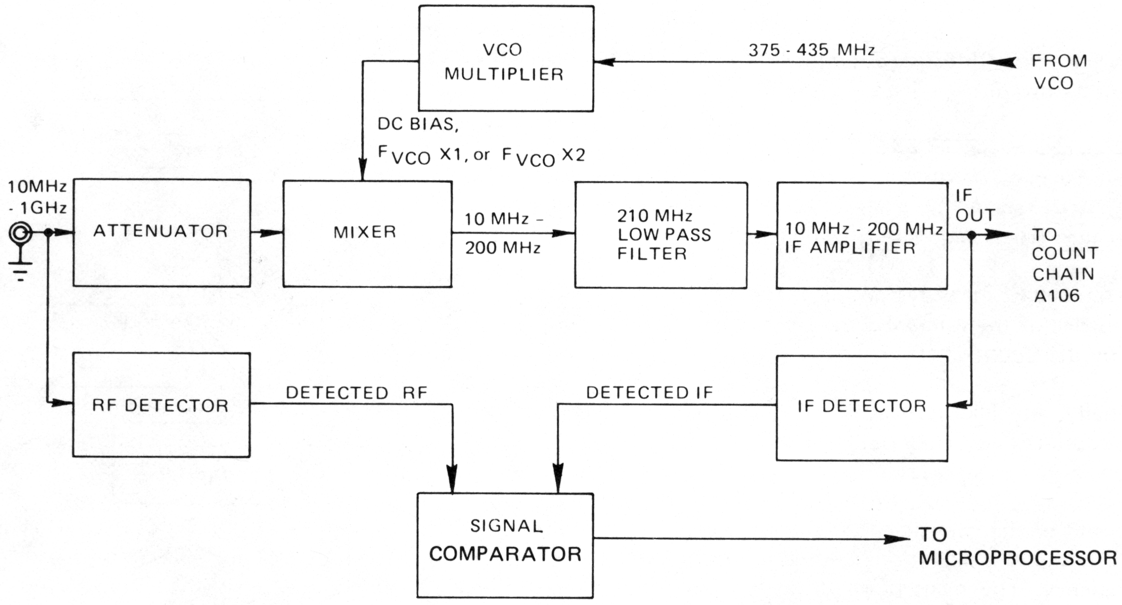

VCO
MULTIPLIER
375 - 435 MHz
FROM VCO
DC BIAS,
F_{VCO} X1, or F_{VCO} X2
10MHz - 1GHz
ATTENUATOR
MIXER
10 MHz - 200 MHz
210 MHz LOW PASS FILTER
10 MHz - 200 MHz IF AMPLIFIER
IF OUT
TO COUNT CHAIN A106
RF DETECTOR
DETECTED RF
DETECTED IF
IF DETECTOR
SIGNAL COMPARATOR
TO MICROPROCESSOR

Figure 4-2 Band 2 Converter Block Diagram, Simplified

The output frequency of the system is the difference between the input signal and the L.O. applied to the mixer. Since the L.O. frequency is a harmonic (N) of the VCO frequency, the unknown input frequency can be expressed as $F_{IN}=N\ F_{VCO} \pm F_{IF}$. There are three primary functions of the software operating the converter:

- To select the appropriate harmonic number N.
- To select an appropriate VCO frequency.
- To determine whether the IF frequency is added to, or subtracted from the L.O. frequency.

These functions are accomplished by selecting N and F_{VCO} and looking for an IF signal of the appropriate amplitude and frequency. Overall system gain is such that whenever the correct L.O. frequency is applied, the IF power will exceed the RF power. This is the primary information used in determining the correct VCO frequency and harmonic number. Once an IF is obtained, the harmonic number is verified and the +/- sign in the equation is determined by shifting the VCO frequency and observing the magnitude and direction of the resulting IF shift. Converter operation is diagrammed in figure 4-3.

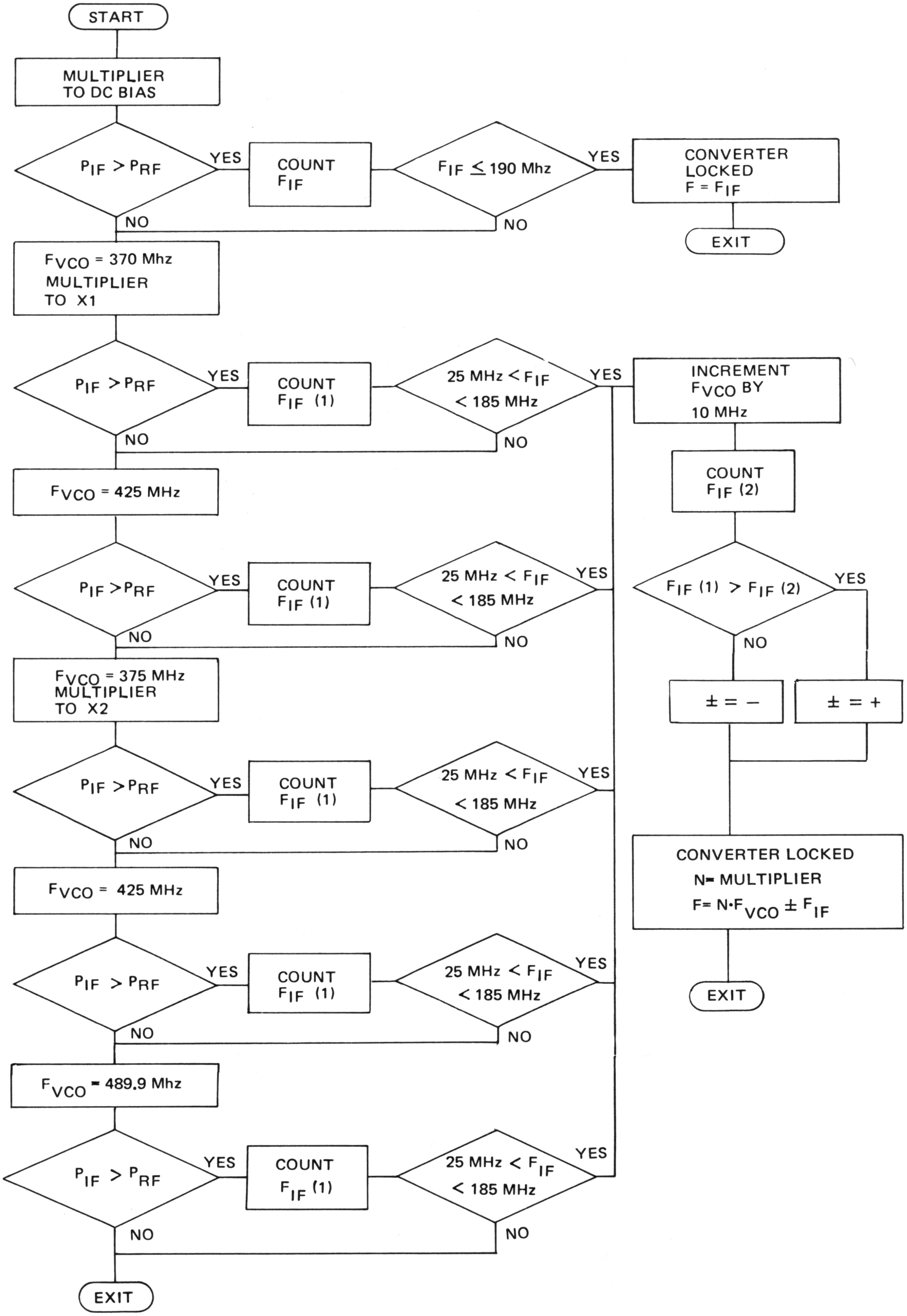

START
MULTIPLIER TO DC BIAS
$P_{IF} > P_{RF}$
YES
NO
COUNT F_{IF}
$F_{IF} \leq 190$ Mhz
YES
NO
CONVERTER LOCKED $F = F_{IF}$
EXIT
$F_{VCO} = 370$ Mhz MULTIPLIER TO X1
$P_{IF} > P_{RF}$
YES
NO
COUNT F_{IF} (1)
25 MHz $< F_{IF} <$ 185 MHz
YES
NO
INCREMENT F_{VCO} BY 10 MHz
COUNT F_{IF} (2)
F_{IF} (1) $> F_{IF}$ (2)
YES
NO
$\pm = -$
$\pm = +$
CONVERTER LOCKED
N= MULTIPLIER
$F = N \cdot F_{VCO} \pm F_{IF}$
EXIT
$F_{VCO} = 425$ MHz
$P_{IF} > P_{RF}$
YES
NO
COUNT F_{IF} (1)
25 MHz $< F_{IF} <$ 185 MHz
YES
NO
$F_{VCO} = 375$ MHz MULTIPLIER TO X2
$P_{IF} > P_{RF}$
YES
NO
COUNT F_{IF} (1)
25 MHz $< F_{IF} <$ 185 MHz
YES
NO
$F_{VCO} = 425$ MHz
$P_{IF} > P_{RF}$
YES
NO
COUNT F_{IF} (1)
25 MHz $< F_{IF} <$ 185 MHz
YES
NO
$F_{VCO} = 489.9$ Mhz
$P_{IF} > P_{RF}$
YES
NO
COUNT F_{IF} (1)
25 MHz $< F_{IF} <$ 185 MHz
YES
NO
EXIT

Figure 4-3. Band 2 Converter Operation

The L.O. frequencies being used, except the range of direct counting (< 190 MHz), have been selected so only IF frequencies from 25 MHz to 185 MHz are required. Since the counter can count signals less than 10 MHz, the restricted operating range provides margin for frequency modulation on the input signal, and for incrementing the VCO frequency.

Figure 4-4 shows the operating ranges for the various harmonics and VCO frequencies used.

Input Frequency Range F_{IN}(MHz)	VCO Frequency F_{VCO}(MHz)	Harmonic Number N	IF Frequency Range F_{IF}(MHz)
10 - 190	—	0	10 - 190
185 - 345	370	1	185 - 25
345 - 400	425	1	80 - 25
400 - 560	375	1	25 - 185
560 - 610	425	1	135 - 185
610 - 725	375	2	140 - 25
725 - 825	425	2	125 - 25
825 - 935	375	2	75 - 185
935 - 1035	425	2	85 - 185
1035 - 1164.8	489.9	2	55.2 - 185

Figure 4-4. Band 2 Operating Ranges

5580021

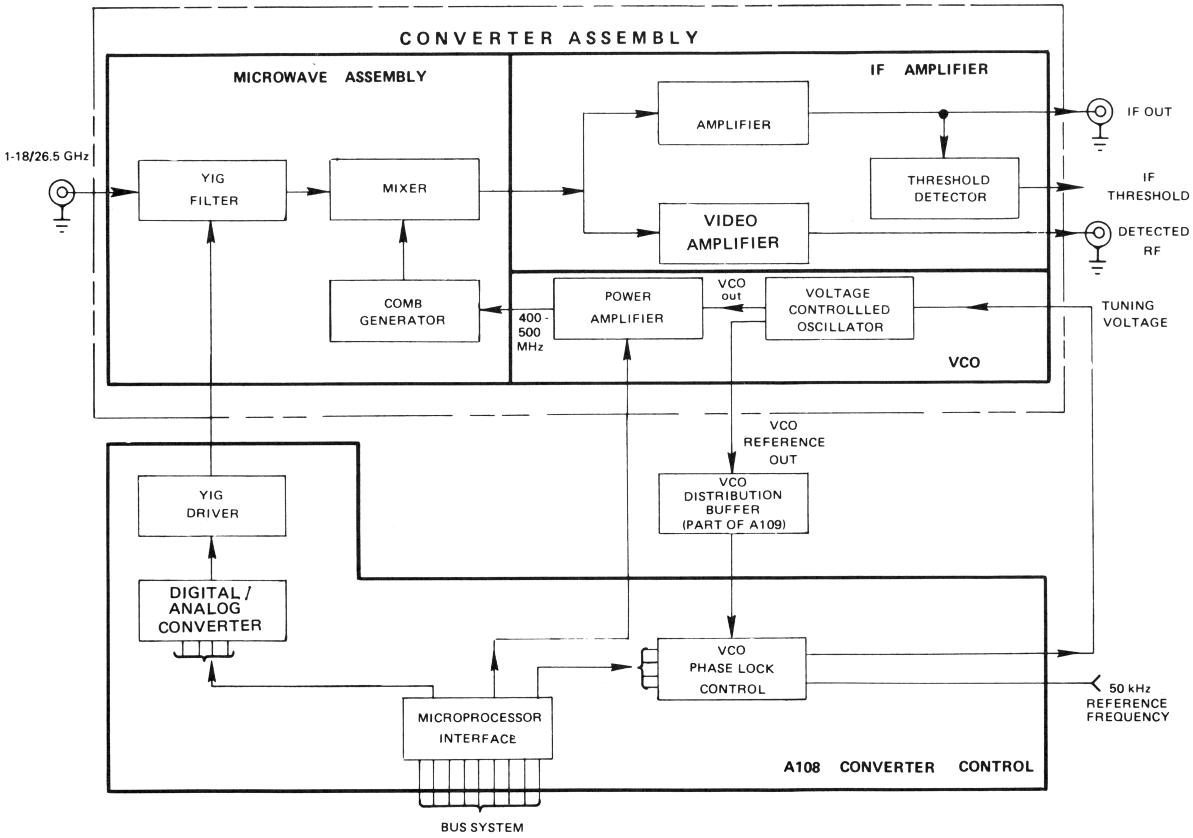

CONVERTER ASSEMBLY
MICROWAVE ASSEMBLY
IF AMPLIFIER
1-18/26.5 GHz
YIG FILTER
MIXER
COMB GENERATOR
AMPLIFIER
VIDEO AMPLIFIER
THRESHOLD DETECTOR
IF OUT
IF THRESHOLD
DETECTED RF
400 - 500 MHz
POWER AMPLIFIER
VCO out
VOLTAGE CONTROLLLED OSCILLATOR
VCO
TUNING VOLTAGE
VCO REFERENCE OUT
YIG DRIVER
VCO DISTRIBUTION BUFFER (PART OF A109)
DIGITAL / ANALOG CONVERTER
VCO PHASE LOCK CONTROL
50 kHz REFERENCE FREQUENCY
MICROPROCESSOR INTERFACE
A108 CONVERTER CONTROL
BUS SYSTEM

Figure 4-5 Band 3 Converter, Simplified.

BAND 3 CONVERTER

Measurement of a signal in Band 3 is accomplished by down converting from the microwave range to approximately 125 MHz. This is accomplished by mixing the input signal with a known reference frequency which is found by selecting a VCO harmonic in the range of 400 to 500 MHz. The VCO frequency can be selected in 50 kHz increments by using a microprocessor controlled phase lock system, while retaining the accuracy and stability of the counter's time base reference.

A simplified diagram of the Band 3 converter is shown in figure 4-5. There are two major assemblies. The Converter Control assembly (A108) and the Converter Assembly (A203).

CONVERTER CONTROL A108

The Converter Control assembly contains the interface between the microprocessor bus system and the Converter (A203). A digital-to-analog converter and a precision current (YIG) driver provide a 2 MHz frequency resolution for setting the YIG filter of A202.

A108 also contains the programmable VCO phase lock control system. This system lets the microprocessor interface select any VCO frequency between 400 and 500 MHz, in increments of 50 kHz.

CONVERTER A203

The Converter assembly consists of three subassemblies.

- A201A, Voltage Controlled Oscillator (VCO) Assembly
- A201B, IF Amplifier Assembly
- A202, Microwave Assembly (yig)

The A202 Microwave Assembly contains the YIG filter, mixer and comb generator.

The input signal (1 GHz - 18 GHz/26.5 GHz) passes through a YIG filter on A202. The filter is an electronically tunable bandpass filter, with an operating frequency proportional to its tuning current. This filter determines the approximate frequency of the input signal, and filters out any undesired signals, making it possible to count a signal at one frequency even if a larger signal is present at another frequency.

When tuning the YIG filter to the input signal, the mixer is used as an RF detector, and its output is amplified in the video amplifier on the IF assembly .

The output of the Video amplifier is maximum when the YIG filter is tuned to the input signal. In the case of multiple input signals, the video amplifier output determines which signal is largest.

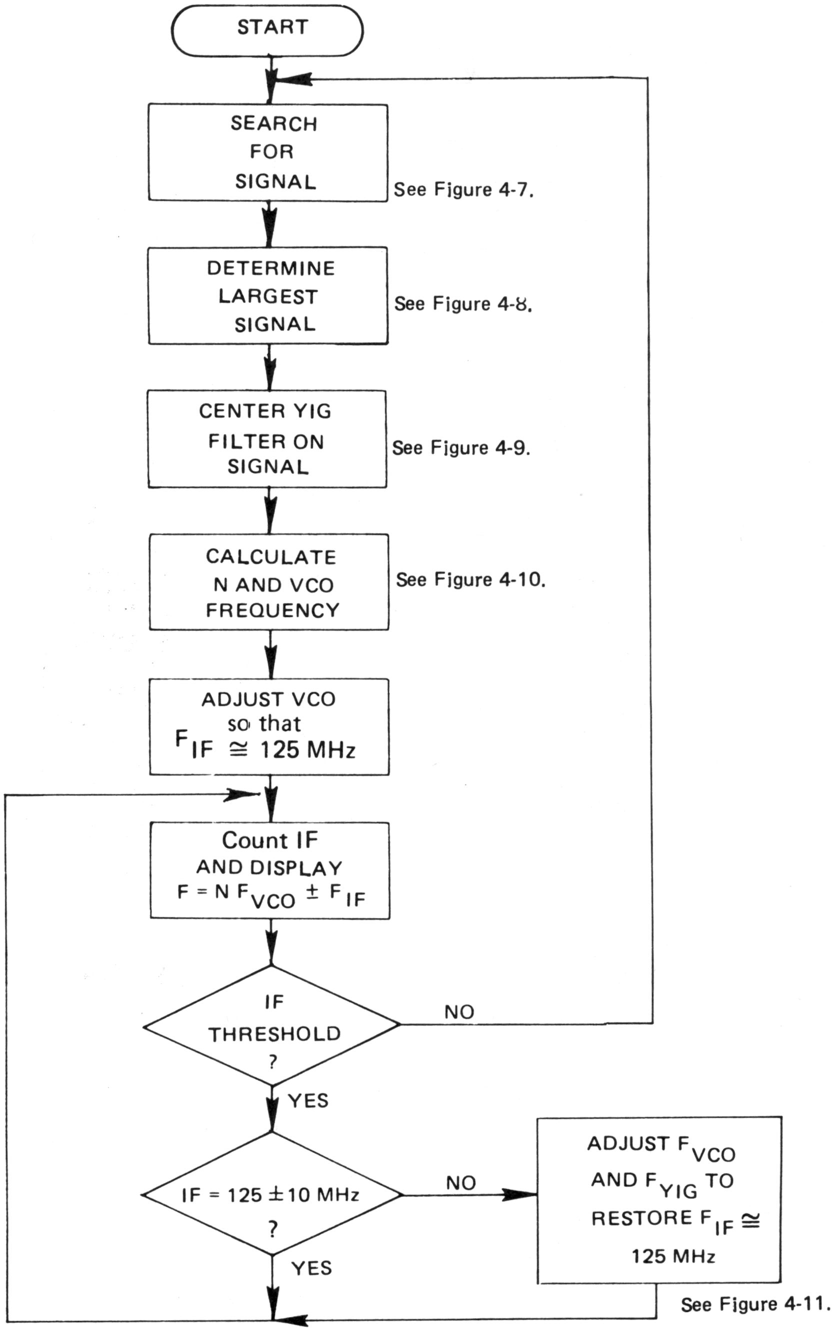

START
SEARCH FOR SIGNAL
See Figure 4-7.
DETERMINE LARGEST SIGNAL
See Figure 4-8.
CENTER YIG FILTER ON SIGNAL
See Figure 4-9.
CALCULATE N AND VCO FREQUENCY
See Figure 4-10.
ADJUST VCO so that $F_{IF} \cong 125$ MHz
Count IF AND DISPLAY $F = N F_{VCO} \pm F_{IF}$
IF THRESHOLD ?
NO
YES
IF = 125 ±10 MHz ?
NO
YES
ADJUST F_{VCO} AND F_{YIG} TO RESTORE $F_{IF} \cong$ 125 MHz
See Figure 4-11.

Figure 4-6. Band 3 Operation, Simplified.

On units equipped with the Power Measurement Option (02), accurate frequency correction factors are stored in the counter's memory. This allows absolute power calibration of the video amplifier output.

Once the YIG filter is tuned to the input signal, the appropriate harmonic number (N) and VCO frequency (F_{VCO}) are selected to produce an IF frequency (F_{IF}) at approximately 125 MHz. An approximation of the input signal is found by using:

$$F_{IN} = N F_{VCO} \pm F_{IF}$$

The IF frequency produced in the mixer is amplified by the high gain IF amplifier and sent to the count chain (A106). The IF threshold detector (A201B) insures sufficient IF amplitude for count accuracy.

OPERATION

First the YIG filter is stepped, (in 64 MHz steps), from its low to high limits. During this search the RF detected output is fed, through a microprocessor controlled step attenuator to a threshold detector. After each step the threshold detector is checked. If triggered, the search mode is halted until the amplitude of the signal is determined. This is done by stepping the filter back and forth through the signal and stepping the attenuator until the signal is attenuated below the threshold. The counter then returns to the search mode to look for any larger signals. After searching the entire frequency range, it returns to the largest signal and begins to center the YIG filter precisely on the input frequency. See Figure 4-6 for a simplified diagram of Band 3 operation. For more detailed descriptions of Band 3 operation see Figures 4-7 through Figure 4-11.

The centering process consists of slowly stepping the YIG filter down (in 2 MHz increments) until a level of 3-6 dB below the peak is reached. This frequency is stored and the process is repeated from the other side by stepping the filter up in 2 MHz steps. The average of the two frequencies obtained is the center of the passband. This is the frequency which is used to determine the N and F_{VCO}.

After centering, N is determined from $N = \frac{F_{YIG} - 125}{500}$ and then rounded up to the next highest integer. From this, F_{VCO} is calculated using $F_{VCO} = \frac{F_{YIG} - 125.}{N}$ Should this yield $F_{VCO} < 400$ MHz, then F_{VCO} is recalculated using $F_{VCO} = \frac{F_{YIG} + 125.}{N}$

Since F_{YIG} is only approximately equal to F_{IN}, the IF frequency will not be exactly 125 MHz. Therefore, the next step in operation is a VCO frequency adjustment to shift F_{IF} into the middle of the IF passband.

VCO frequency correction is achieved by counting F_{IF} and changing F_{VCO} by $\pm \frac{F_{IF} - 125.}{N}$ If the error is large enough to be outside the IF passband (IF threshold is not triggered) then a series of steps (shifting the IF in ± 20 MHz increments) are taken until the signal falls within the passband.

Once the VCO corrections have been made, the converter has acquired the signal and the counter is ready to count and display the input frequency.

After each measurement, the frequency of the IF is examined. If the input frequency has shifted more than 10 MHz, new frequencies for the YIG and VCO are calculated to restore the IF to 125 MHz. This method provides rapid tracking of a signal being tuned.

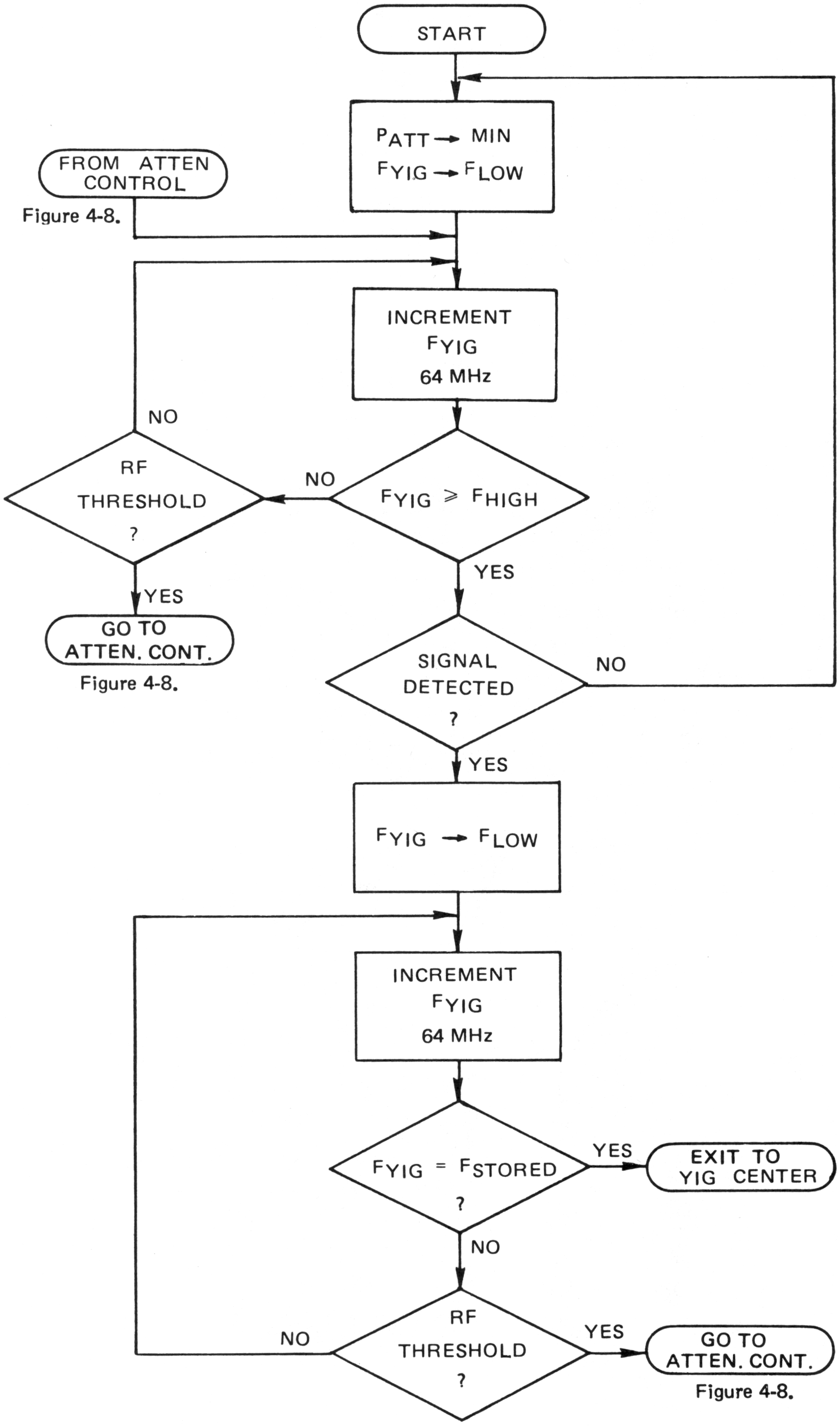
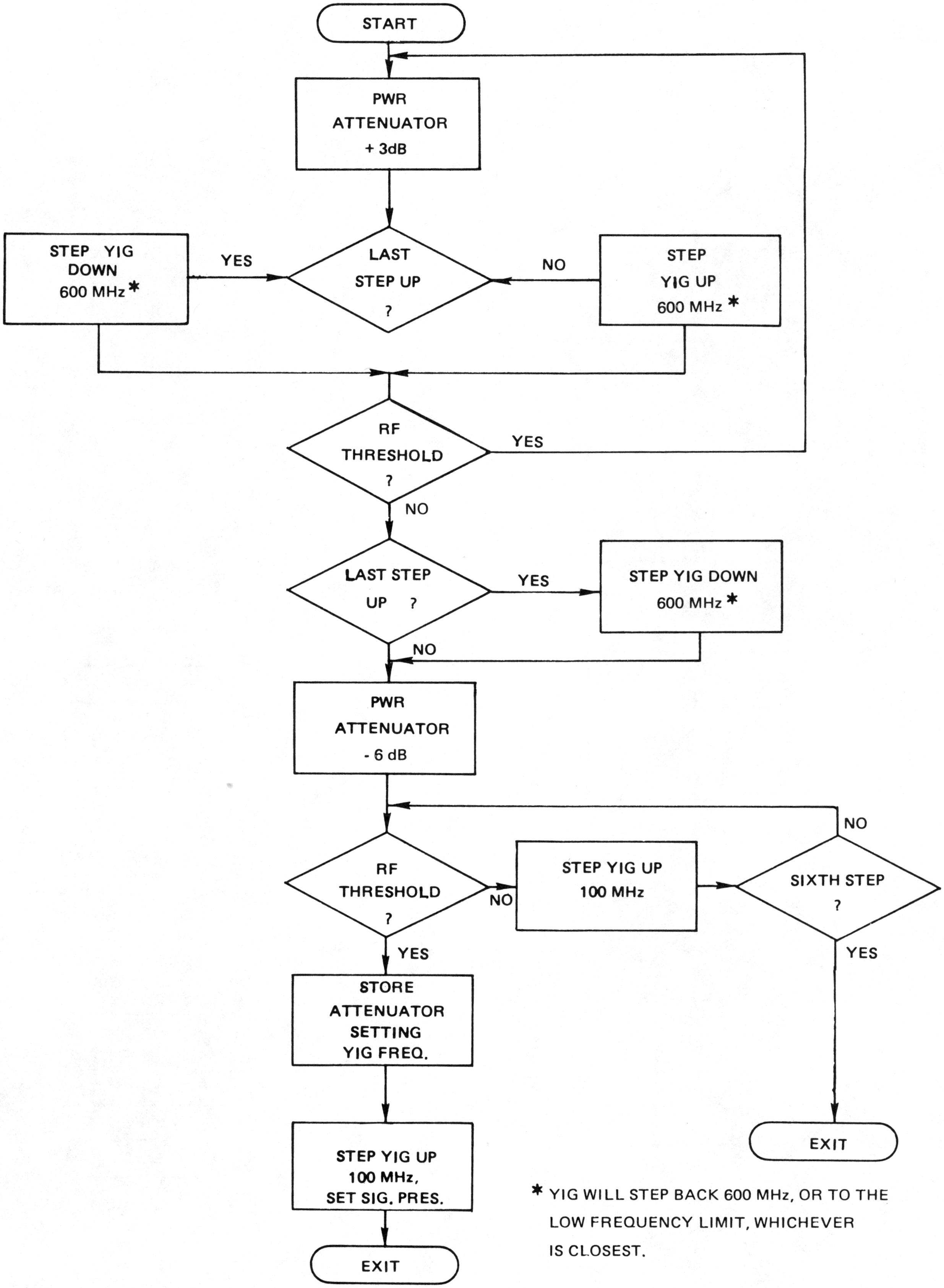

START
PATT → MIN
FYIG → FLOW
FROM ATTEN CONTROL
Figure 4-8.
INCREMENT FYIG 64 MHz
NO
RF THRESHOLD ?
NO
FYIG ⩾ FHIGH
YES
YES
GO TO ATTEN. CONT.
Figure 4-8.
SIGNAL DETECTED ?
NO
YES
FYIG → FLOW
INCREMENT FYIG 64 MHz
FYIG = FSTORED ?
YES
EXIT TO YIG CENTER
NO
RF THRESHOLD ?
NO
YES
GO TO ATTEN. CONT.
Figure 4-8.

Figure 4-7. Band 3 Search For Signal


START
PWR
ATTENUATOR
+ 3dB
STEP YIG
DOWN
600 MHz *
YES
LAST
STEP UP
?
NO
STEP
YIG UP
600 MHz *
RF
THRESHOLD
?
YES
NO
LAST STEP
UP ?
YES
STEP YIG DOWN
600 MHz *
NO
PWR
ATTENUATOR
- 6 dB
NO
RF
THRESHOLD
?
NO
STEP YIG UP
100 MHz
SIXTH STEP
?
YES
YES
STORE
ATTENUATOR
SETTING
YIG FREQ.
EXIT
STEP YIG UP
100 MHz,
SET SIG. PRES.
EXIT

* YIG WILL STEP BACK 600 MHz, OR TO THE LOW FREQUENCY LIMIT, WHICHEVER IS CLOSEST.

Figure 4-8. Determine Largest Signal

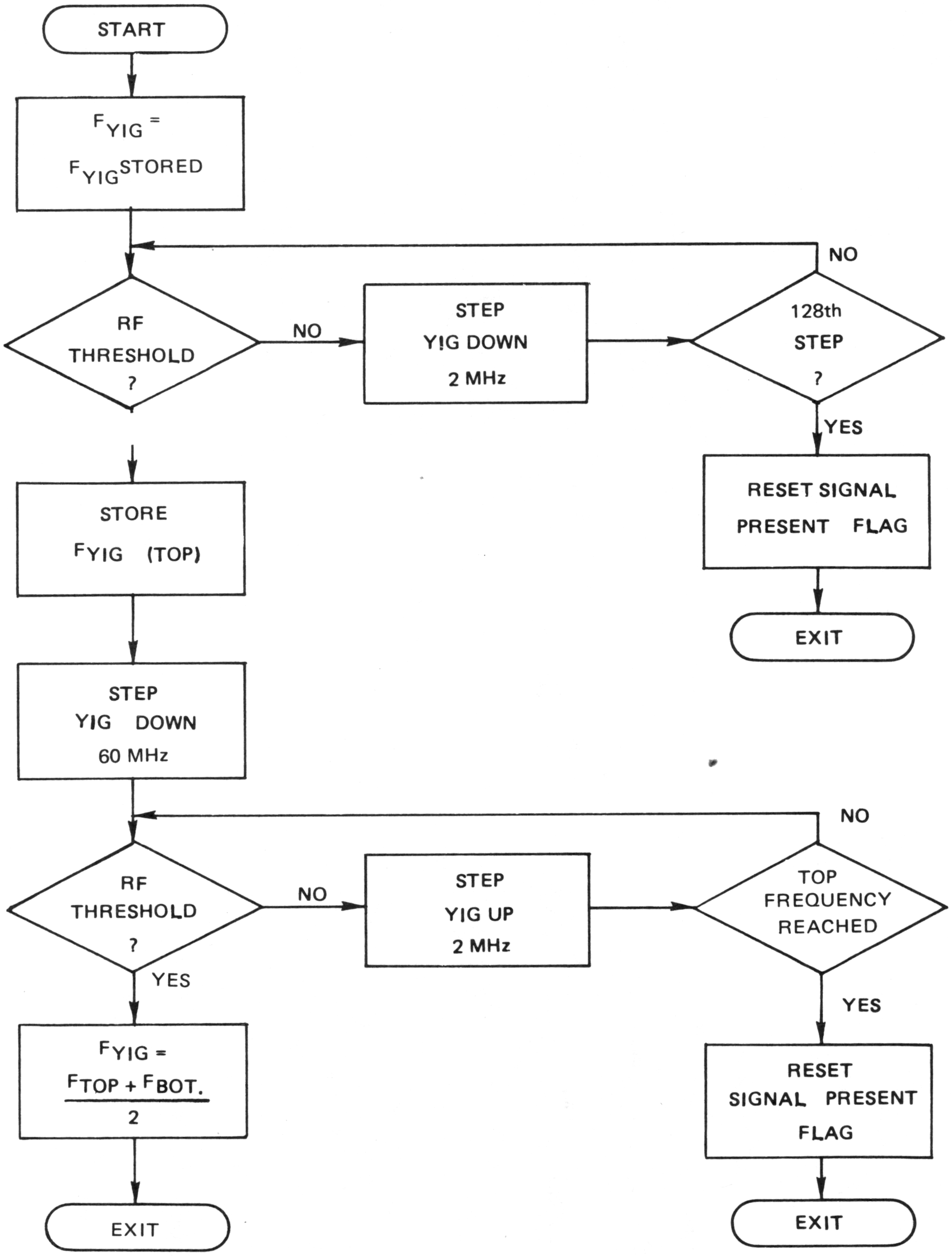

START
FYIG =
FYIGSTORED
RF
THRESHOLD
?
NO
STEP
YIG DOWN
2 MHz
128th
STEP
?
NO
YES
RESET SIGNAL
PRESENT FLAG
EXIT
STORE
FYIG (TOP)
STEP
YIG DOWN
60 MHz
RF
THRESHOLD
?
NO
STEP
YIG UP
2 MHz
TOP
FREQUENCY
REACHED
NO
YES
RESET
SIGNAL PRESENT
FLAG
EXIT
YES
FYIG =
FTOP + FBOT.
2
EXIT

Figure 4-9. YIG Centering

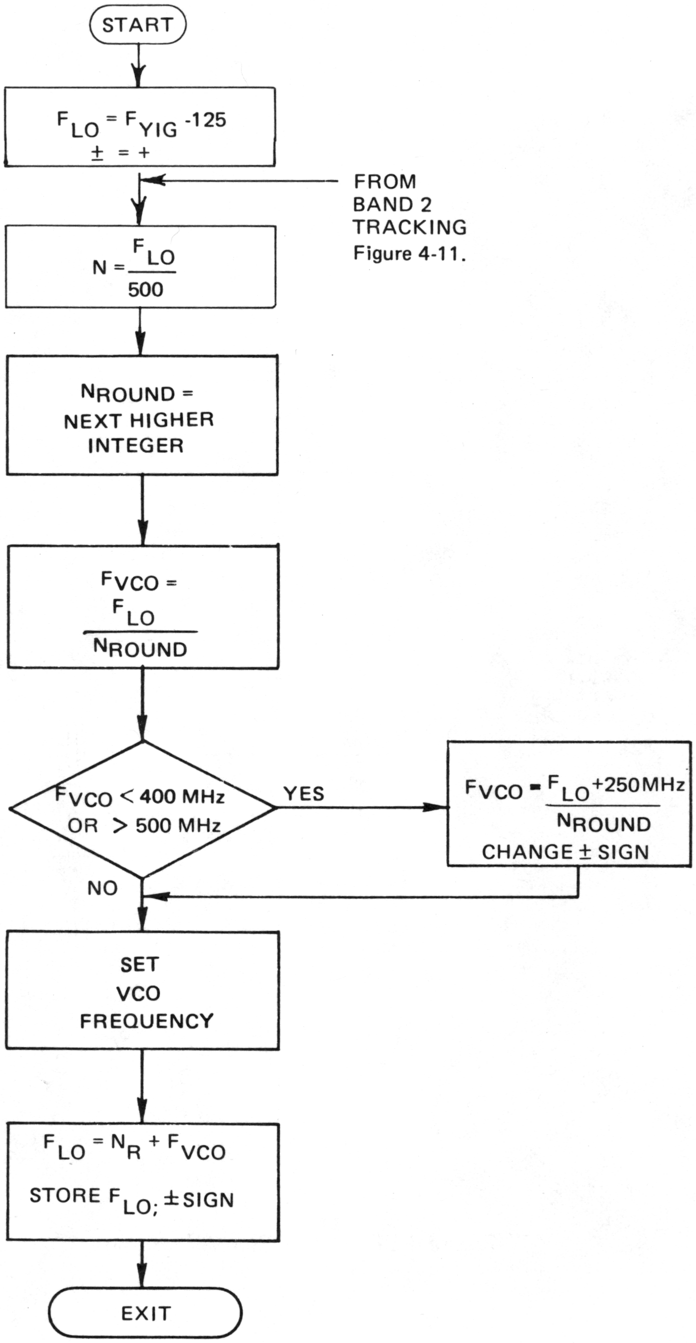

START
FLO = FYIG -125
± = +
FROM
BAND 2
TRACKING
Figure 4-11.
N = FLO / 500
NROUND =
NEXT HIGHER
INTEGER
FVCO =
FLO / NROUND
FVCO < 400 MHz
OR > 500 MHz
YES
NO
FVCO = FLO+250MHz / NROUND
CHANGE ± SIGN
SET
VCO
FREQUENCY
FLO = NR + FVCO
STORE FLO; ±SIGN
EXIT

Figure 4-10. Calculate N and VCO Frequency

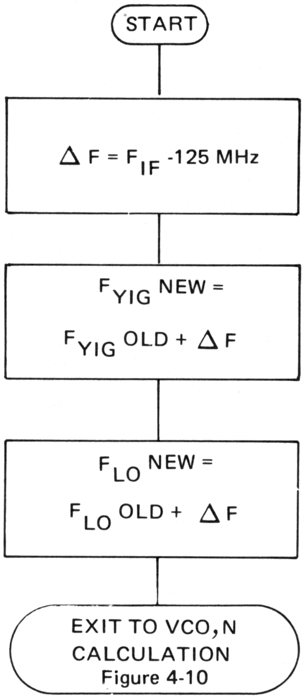

START
ΔF = F_IF -125 MHz
F_YIG NEW =
F_YIG OLD + ΔF
F_LO NEW =
F_LO OLD + ΔF
EXIT TO VCO, N
CALCULATION
Figure 4-10

Figure 4-11. Band 3 Signal Tracking

Section 5
Maintenance and Service

This section contains instructions and information to maintain your counter.

FUSE REPLACEMENT

The counter uses one fuse. It is located on the rear panel next to the voltage select switch.

- For 100/120VAC operation use a 1.0A slow-blow MDL type fuse.
- For 220/240VAC operation use a 0.50A slow-blow FST type fuse.

The voltage select switch should be set to the proper line voltage. To change line voltage:

1. Be sure the counter is disconnected from the power line.
2. With a flat edged screwdriver, rotate the voltage select switch until the arrow points to the desired line voltage.
3. Change to a fuse with the value specified for the line voltage selected.

NOTE:
Always be sure that the fuse is the type and value specified for, and that the voltage select switch is set to correspond to the AC power input voltage, or the counter may be damaged.

AIR CIRCULATION

Air circulates through the vents in the rear panel of the counter. These vents must not be obstructed or the temperature inside the counter may increase enough to reduce the counter stability and shorten the component life.

PERIODIC MAINTENANCE

No periodic preventive maintenance is required. To maintain accuracy, it is recommended that the counter be recalibrated every six months.

CAUTION

Do not attempt repair or disassembly of the Microwave Converter or Time Base Oscillator Assemblies. Contact EIP or your sales representative.

If the following assemblies are repaired or replaced the counter may require recalibration for proper operation.

- Power Supply, A101
- Gate Generator, A107
- Converter Control, A108
- Microwave Converter, A203

Care should be taken when removing any assemblies to prevent damage to components or cables.

FACTORY

If the counter is being returned to EIP for service or repair, be sure to include the following information with the shipment.

- Name and address of owner.
- Model and complete serial number of counter.
- A COMPLETE description of problem (Under what conditions did problem occur? What was the signal level? What equipment was attached or connected to the counter? Did that equipment experience failure symptons?)
- Name and telephone number of someone familiar with the problem that may be contacted by EIP for any further information, if necessary.
- Shipping address to which the counter is to be returned. Include any special shipping instructions.
- Pack the counter for shipping (Refer to Section 2).

FIELD

EIP has an assembly exchange program. All plug in assemblies, modules, and the front panel assembly may be exchanged.

After identifying the faulty assembly, call EIP with the assembly number and shipping information. A replacement will be shipped within 24 hours. After the replacement assembly has been received, return the faulty assembly to EIP for credit.

Section 6
Troubleshooting

This section defines troubleshooting aids that are incorporated in the 545A/548A counter. They are:

- Signature analysis
- Self diagnostics
- Keyboard controlled circuit tests

The procedures and tables are provided for troubleshooting to a functional circuit level.

SIGNATURE ANALYSIS

Signature analysis is a technique used to troubleshoot complex logic circuitry. It uses data compression to reduce any data pattern to a 4 character alpha-numeric word.

The start and stop inputs define the measurement window. Each time a transition within the measurement window occurs on the clock input, the probe is sampled, and the logic level is shifted into the analyzer. This information is used to generate a signature unique to that data string. That signature can then be compared to a reference signature, taken from a known good product, to determine if the data string is correct.The counter implements signature analysis in either a free running or program controlled manner.

FREE RUNNING

This mode of signature analysis is essential for troubleshooting problems that could prevent the program from running. A CLRB instruction can be forced by breaking the data bus at A105 JMP1 and grounding A105 TP5, effectively "free running" the microprocessor. "Free running" means forcing a simple instruction (such as NOP or CLRB) on the data bus, which the microprocessor sees at every address location. This causes the microprocessor to continually cycle through its entire address range, accessing everything on the address bus as it does. By strategically placing the start and stop connections the entire bus system can be probed for bad signatures.

	START	STOP	CLOCK
CONNECTIONS	A105 TP2	A105 TP2	A105 TP8
BUTTONS	IN	IN	IN

LINE	SIGNATURE	LINE	SIGNATURE
A0 (P1 Pin 54)	UUUU	U8 Pin 8	9UPO
A1 (P1 Pin 54)	FFFF	12	755P
A2 (P1 Pin 52)	8484	U11 Pin 2	9UP1
A3 (P1 Pin 51)	P763	4	4FCA
A4 (P1 Pin 50)	1U5P	6	37C5
A5 (P1 Pin 49)	0356	8	7791
A6 (P1 Pin 48)	U759	11	6321
A7 (P1 Pin 47)	6F9A	13	6U28
A8 (P1 Pin 46)	7791	15	4868
A9 (P1 Pin 45)	6321	17	00001
A10 (P1 Pin 44)	37C5	U12 Pin 2	U759
A11 (P1 Pin 43)	6U28	4	1U5P
A12 (P1 Pin 42)	4FCA	6	8484
A13 (P1 Pin 41)	4868	8	UUUU
A14 (P1 Pin 40)	9UP1	11	FFFF
A15 (P1 Pin 39)	00001	13	P763
U1 Pin 5	0003	15	0356
U2 Pin 9	75HA	17	6F9A
U4 Pin 2	6U2C	U18 Pin 4	6H4C
8	9UP3	5	0994
10	9UP2	6	U3H7
12	0002	7	P257
U5 Pin 6	755F	9	854F
8	PACU	10	H602
12	0003	11	25P6
		12	9F14

+ 5V 0003, phase 2 0003 *

* Due to the synchronous qualities of the signature analyzer, phase 2 will read the same as + 5V but the logic probe will be flashing. Likewise, anything gated with phase 2 may have the same signature as the ungated signal.

Figure 6-1. Microprocessor Free Running Signatures

	START	STOP	CLOCK
CONNECTIONS BUTTONS	A105 TP14 IN ↓	A105 TP15 OUT ↑	A105 TP8 IN ↓

NODE	SIGNATURE	NODE	SIGNATURE
A105 JMP1 Pin 9	8HU1	A105 JMP1 Pin 13	C38U
A105 JMP1 Pin 10	7068	A105 JMP1 Pin 14	CU8P
A105 JMP1 Pin 11	F439	A105 JMP1 Pin 15	7096
A105 JMP1 Pin 12	U774	A105 JMP1 Pin 16	3H73
+5V	1817		

Figure 6-2. Signatures, Basic PROM Set

PROGRAM CONTROLLED

If the counter is working sufficiently to access the test functions, program controlled signature analysis can be used. In program controlled signature analysis the start and stop (and therefore the signature) are controlled by software. This allows the signature analyzer to be used, in many cases, to troubleshoot the hardware outside the bus system.

SELF DIAGNOSTICS

At turn on the counter performes several internal diagnostic checks, checking the RAM, PROM, and the associated decoding circuitry. The display shows dashes during these checks. If the counter passes the tests it then enters the normal operating mode. If it fails RAM check the display will show all Es and a unique signature will be generated. If the counter fails any of the PROM checks an error message will be displayed, and a signature will be generated. Please refer to figure 6-3.

The counter generates PROM error signatures only during the power up diagnostics check. It is necessary to turn the power off, and then on again, while the signature analyzer is connected, to get a signature.

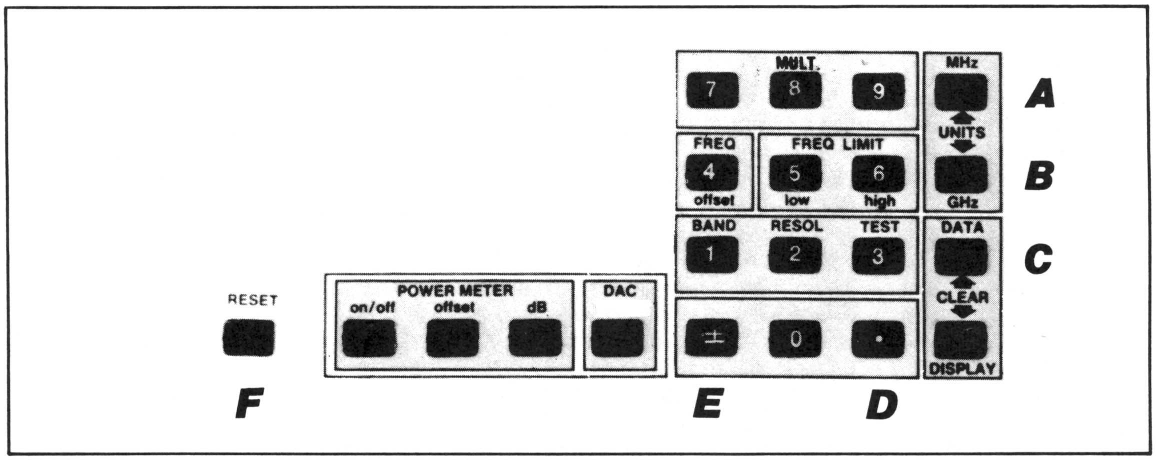
	START	STOP	CLOCK	PROBE
CONNECTION BUTTONS	A106 TP5 OUT ↑	A106 TP5 IN ↓	A105 TP8 IN ↓	A105 TP6 (+5V)

PROBLEM	ERROR	SIGNATURE
Ram Bad	All E's	007U
A105 U13 (Basic Program) Bad	31	1UFP
A105 U17 (Basic Program) Bad	32	U399
A105 U15 (Basic Program) Bad	33	P672
A107 U2 (Power Meter) Bad	34	9FA8
A105 U14 (Band 4) Bad	35	2A2C
A105 U17 (GPIB or BCD/RMT) Bad	36	8AFH

Figure 6-3. Self Diagnostic Error Indications

KEYBOARD CONTROLLED CIRCUIT TESTS

There are 11 keyboard controlled circuit tests (01 thru 11). All tests are accessed by pressing TEST ☐ and then the two digit test number. Tests which do not require keyboard inputs to function (tests 01, 02, 03, 04, 06, 07, 11) can be exited by pressing any key. The counter will exit the test and enter the functions selected. Tests which use the keyboard in their operation (tests 05, 08, 09, 10) can be exited by pressing any key not used by the test. All tests can be exited by pressing CLEAR ☐ DISPLAY. The counter will return to normal operation. Some tests require hexidecimal coded keyboard inputs (tests 08, 09, 10). For those tests the keyboard is defined in figure 6-4.


MULT.
7
8
9
MHz
A
UNITS
FREQ
4
offset
FREQ LIMIT
5
low
6
high
B
GHz
BAND
1
RESOL
2
TEST
3
DATA
C
RESET
POWER METER
on/off
offset
dB
DAC
±
0
•
CLEAR
DISPLAY
F
E
D

KEY	HEX EQUIV.	KEY	HEX EQUIV.
0	0	9	9
1	1	MHz	A
2	2	GHz	B
3	3	CLR DATA	C
4	4		
5	5	●	D
6	6	+/–	E
7	7	RESET	F
8	8	CLR DISPLAY	EXITS TEST

Figure 6-4. Keyboard Configuration For Tests Requiring Hexidecimal Inputs.

	START	STOP	CLOCK	PROBE
CONNECTION	OUT ↑	IN ↓	IN ↓	
BUTTONS	A106 TP5	A106 TP5	A105 TP8	A105 TP6 (+5V)

BUTTON	COORDINATES	SIGNATURE
Reset	47	U68C
Power ON/OFF	46	U7HA
Power Offset	36	20P6
dB	16	U2F9
DAC	26	811P
7	41	A19C
8	42	66PU
9	43	CCH7
MHz	44	U5PU
4	31	PUPH
5	32	UC70
6	33	HF3A
GHz	34	OPA2
1	21	APH1
2	22	C45H
3	23	1766
CLR DATA	24	H9C8
+/–	11	375U
0	12	H7PC
●	13	UAHH
CLR DISPLAY	EXIT TEST	C75U

Figure 6-5. Keyboard Test Coordinates and Signatures.

TESTS

01 **200 MHz Self Test** This test sets the VCO to 400 MHz, divides it by two, and counts the 200 MHz output from the divider. It checks the count chain, VCO and VCO phase lock circuitry, and the gate generator.

02 **8's Test** This will light all LED's, annunicators, and decimal points. It checks that everything on the display is lit, the intensity of the display, and the alignment of the LED's and annunciators.

03 **Display Segment Test** This lights one segment of each digit, and one annunciator at a time, cycling through all segments. The cycle rate can be adjusted with the sample rate pot. It verifies that each segment of the display, segment drivers and display multiplexer, operate properly and independently.

04 **Display Digit Test** This lights one entire digit, and its decimal point, at a time. It cycles through all digits and annunciators. The cycle rate is determined by the sample rate pot. It checks each digit and digit driver independently, and verifies operation of the display multiplexer.

05 **Keyboard Test** This will display the coordinates of each key as it is pressed. It also generates a unique signature for each key, so the keyboard can be checked without the display. Test 05 may be entered by keyboard or by momentarily tying A108 TP1 to A105 TP8 (or to A108, U5, pin 25). This makes it possible to enter the keyboard test for troubleshooting even if the keyboard is not operating well enough to enter the test in a normal manner. Test 05 checks the keyboard, keyboard interrupt, and keyboard decode circuitry. The coordinates and signatures for each key are shown in figure 6-5.

06 **Converter Ramp Test** Test 06 continuously ramps the Band 3 Converter DAC from 0 to 27 GHz, in 2 MHz (LSB) steps. It also generates a signature for each of the inputs to the DAC. (See figure 6-6). It can be used to test the yig DAC, yig drivers, yig, and Band 3 RF level circuits.

	START	STOP	CLOCK	PROBE
CONNECTIONS	A106 TP5	A106 TP5	A105 TP8	A105 TP6 (+5V)
BUTTONS	OUT ↑	IN ↓	IN ↓	

NODE	SIGNATURE	NODE	SIGNATURE
A108 U5 Pin 2	2694	A108 U5 Pin 9	077F
A108 U5 Pin 3	8792	A108 U5 Pin 10	A3H5
A108 U5 Pin 4	5287	A108 U5 Pin 11	28PU
A108 U5 Pin 5	P082	A108 U5 Pin 12	7180
A108 U5 Pin 6	P588	A108 U5 Pin 13	U577
A108 U5 Pin 7	2HU2	A108 U5 Pin 14	F979
A108 U5 Pin 8	UPFO	A108 U5 Pin 15	7823
+ 5V	8142		

Figure 6-6. Converter Ramp Test Signatures

07 **VCO Test** This test cycles the VCO frequency from 400 to 500 MHz, in increments of 500 kHz. The cycle rate can be adjusted by the sample rate pot. 07 tests the VCO and the phase lock circuitry.

08 **Power Meter Offset Test** This makes it possible to set the power meter zero DAC to any setting. The setting is entered as a four digit hexidecimal number (figure 6-6). The first two digits are used to program the course offset DAC, and the last two digits program the fine offset DAC. Test 08 enables the power meter zero DAC to be tested, and can provide a DC level signal to aid in testing the power meter circuit.

09 **Power Meter Gain Test** This makes it possible to set the power meter sensing circuit to any number. The number is entered as a five digit hexidecimal number (figure 6-6) in the following format.

1st digit	A107 U10 bits 4-7
2nd digit	A107 U10 bits 0-3
3rd digit	A107 U12 bits 4-7 (Power Meter Option only)
4th digit	A107 U12 bits 0-3 (Power Meter Option only)
5th digit bit 0	Sets Amp marked "15 dB Gain" to high gain
5th digit bit 1	Sets Amp marked "30 dB Gain" to high gain

Digit 5 is a 2 bit number, so any number entered for digit 5 will be justified to a number from 0-3. Test 09 checks the RF level and power meter circuits.

10 **Information Read/Alter Routine** Test 10 can read any microprocessor address and, if that address is RAM or I/O, change its contents. The desired address is entered as a 4 digit hexidecimal number (see figure 6-6). When the 4th digit is entered the counter will display the contents of the desired address. The contents are then changed by entering a two digit hexidecimal number.

NOTE

Test 10 can change any temporary storage in the counter, including locations that are essential to the operation of the counter. Changing the wrong location will not damage the counter permanently, but it can cause improper operation. To return the counter to proper operation turn the counter off then back on.

11 Test 11 for the DAC option 01 is described in Section 10.

SIGNIFICANT ADDRESSES, I/O PORTS

If an I/O bit is configured as an output, the number read by test 10 will be the same number that is programmed. If an I/O bit is configured as an input, the number read by test 10 will be the input signal level on the I/O line. Therefore, if an I/O port is programmed, and then read, the number displayed may not correspond to the number programmed because some bits of the I/O port may be configured as inputs.

DESCRIPTION	ADDRESS OF PA PORTS	ADDRESS OF PB PORTS
PIA on Count Chain (A106)	AC00	AC02
PIA on Gate Generator (A107)	9900	9902
Frequency Control PIA on Converter Control A108	9840	9842
Programmable Counter PIA on Converter Control (A108)	9820	9822
PIA on Band 2 Converter (A109)	9880	9882
PIA on Front Panel Logic (A111)	9808	980A
PIA on BCD/Remote (A102)	9A00	9A02
PIA on DAC Board (A103)	A820	A822

DESCRIPTION	ADDRESS
GPIB Address Switch	9C04

Figure 6-7. I/O Addresses.

Two important I/O port locations are the yig frequency control (address 9840, 9842) and the FCO frequency control (address 9820, 9822).

To convert from the desired yig frequency to the PIA program number:

1. Round the desired frequency to a multiple of 2 MHz (The yig DAC resolution is 2 MHz).
2. Divide the desired frequency in MHz by 2 (F/2).
3. Convert F/2 from decimal to hexidecimal.
4. The two most significant digits are programmed to address 9842, and the two least significant digits are programmed to address 9840.

To convert from the desired VCO frequency to the PIA program number:

EXAMPLE (420. 75 MHz)

1. Round the desired frequency to a multiple of 50 kHz
   (The resolution of the VCO frequency is 50 kHz).
2. Multiply the desired frequency (in MHz) by 5. . . . . 420. 75 X 5 = 2103.75
3. If the result contains no fractional part, go to step 8.
4. Multiply only the fractional part by 16 . . . . .75 X 16 = 12
5. Add the result to the most significant digit from step 2. . . . . MSD of 2103.75 = 2 - 2 + 12 = 14
6. Convert the result to hexidecimal . . . . $14_{10} = E_{16}$
7. Replace the MSD from step 2 with the result from step 6
   and drop the fractional part. . . . . 2103.75 → E103
8. The two most significant digits are programmed to address 9822, and the two least significant digits are programmed to address 9820.

SIGNIFICANT ADDRESSES, RAM

All storage in RAM are in the following formats.

REGISTER FORMAT, FREQUENCY STORAGE			REGISTER FORMAT, POWER STORAGE		
ADDRESS	SIGN (00 = + , FF = –)		ADDRESS	SIGN (00 = +, FF = –)	
ADDRESS + 1	100 GHz	10 GHz	ADDRESS + 1	NOT	USED
ADDRESS + 2	1 GHz	100 MHz	ADDRESS + 2	NOT	USED
ADDRESS + 3	10 MHz	1 MHz	ADDRESS + 3	NOT	USED
ADDRESS + 4	100 KHz	10 KHz	ADDRESS + 4	NOT	USED
ADDRESS + 5	1 KHz	100 Hz	ADDRESS + 5	100 dB	10 dB
ADDRESS + 6	10 Hz	1 Hz	ADDRESS + 6	1 dB	. 1 dB

REGISTER	ADDRESS
L.O. frequency	01A8
I.F. frequency	023F
Frequency output to display	01B8
Frequency limit low	025B
Frequency limit high	0254
Frequency offset	0246

Figure 6-8. Frequency Storage Registers

REGISTER	ADDRESS
Power output to display	01BF
Power offset	024D

Figure 6-9. Power Storage Registers

TROUBLESHOOTING TREES

Troubleshooting trees are intended only as a guide, and do not describe every possible failure situation. Turn power off before removing or installing any P.C. boards or connectors. If the following assemblies are repaired or replaced, recalibration of the counter will be necessary.

- A101 Power Supply
- A107 Gate Generator
- A108 Converter Control
- A203 Converter Assembly

CAUTION

Do not attempt to repair or disassemble
the A203 hybrid assembly.

TEST EQUIPMENT REQUIRED

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
Tektronix	475	Oscilloscope	100 MHz min. Bandwidth
Fluke	8050A	D.V.M.	4½ digit resolution
H.P.	182C, 8559A	Spectrum Analyzer	125 MHz
H.P.	5004A	Signature Analyzer	
H.P.	651B	Signal Generator	10 Hz - 10 MHz
Wavetek	2002	Sweeper	10 MHz - 2 GHz
Wiltron	610D, 6237D	Microwave Sweeper	2 GHz - 18 GHz
H.P.	8690A, 8696A	Microwave Sweeper	18 GHz - 26. 5 GHz

Figure 6-10. Troubleshooting Test Equipment (Or Equivalent).

To use the troubleshooting trees:

1. Refer to the main troubleshooting tree.
2. Step through the main troubleshooting tree, performing all necessary checks, until the failure mode is noted.
3. Refer to the appropriate troubleshooting tree for that failure mode.

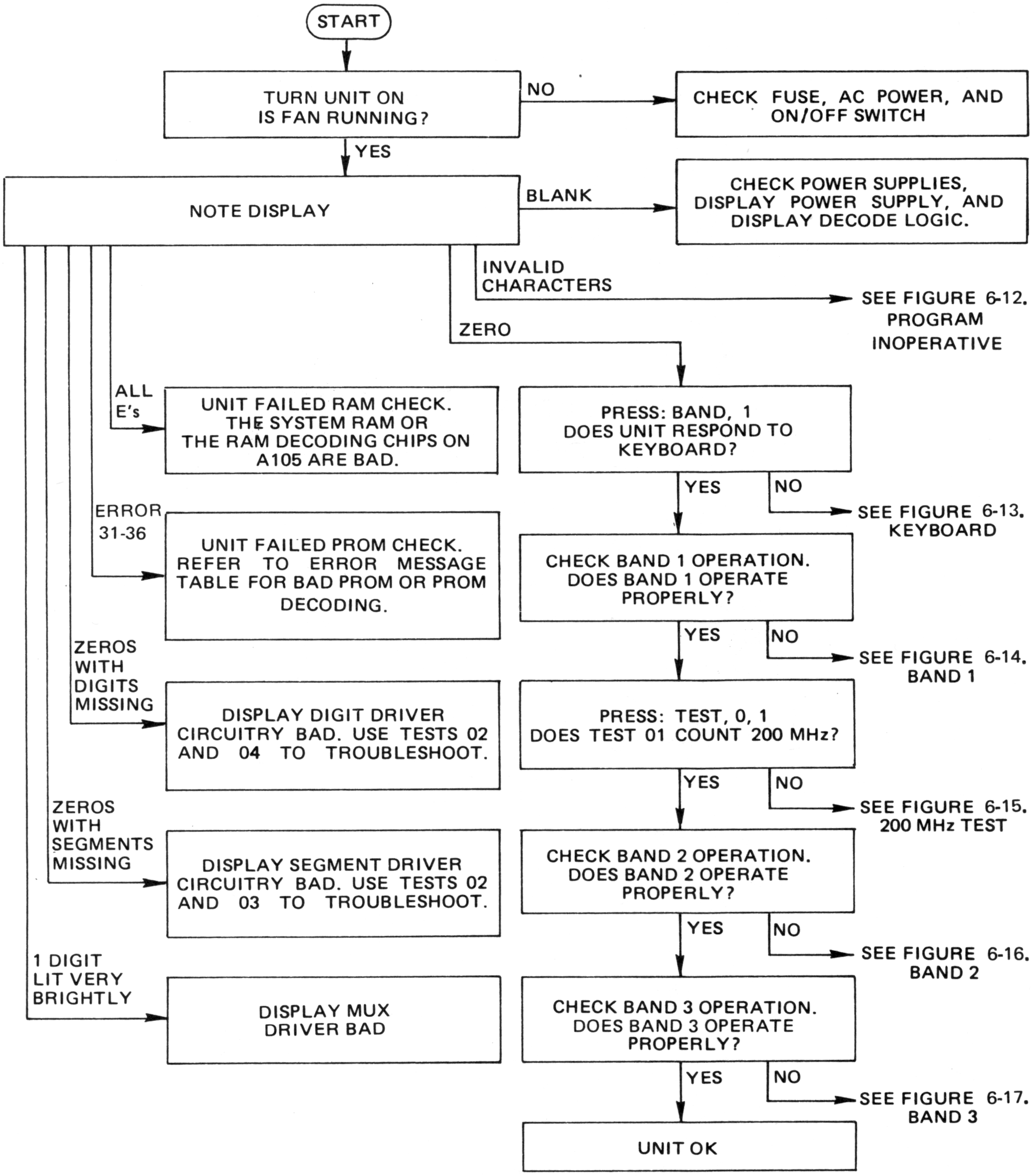

START
TURN UNIT ON
IS FAN RUNNING?
NO
CHECK FUSE, AC POWER, AND ON/OFF SWITCH
YES
NOTE DISPLAY
BLANK
CHECK POWER SUPPLIES, DISPLAY POWER SUPPLY, AND DISPLAY DECODE LOGIC.
INVALID CHARACTERS
SEE FIGURE 6-12. PROGRAM INOPERATIVE
ZERO
ALL E's
UNIT FAILED RAM CHECK. THE SYSTEM RAM OR THE RAM DECODING CHIPS ON A105 ARE BAD.
PRESS: BAND, 1
DOES UNIT RESPOND TO KEYBOARD?
YES
NO
SEE FIGURE 6-13. KEYBOARD
ERROR 31-36
UNIT FAILED PROM CHECK. REFER TO ERROR MESSAGE TABLE FOR BAD PROM OR PROM DECODING.
CHECK BAND 1 OPERATION. DOES BAND 1 OPERATE PROPERLY?
YES
NO
SEE FIGURE 6-14. BAND 1
ZEROS WITH DIGITS MISSING
DISPLAY DIGIT DRIVER CIRCUITRY BAD. USE TESTS 02 AND 04 TO TROUBLESHOOT.
PRESS: TEST, 0, 1
DOES TEST 01 COUNT 200 MHz?
YES
NO
SEE FIGURE 6-15. 200 MHz TEST
ZEROS WITH SEGMENTS MISSING
DISPLAY SEGMENT DRIVER CIRCUITRY BAD. USE TESTS 02 AND 03 TO TROUBLESHOOT.
CHECK BAND 2 OPERATION. DOES BAND 2 OPERATE PROPERLY?
YES
NO
SEE FIGURE 6-16. BAND 2
1 DIGIT LIT VERY BRIGHTLY
DISPLAY MUX DRIVER BAD
CHECK BAND 3 OPERATION. DOES BAND 3 OPERATE PROPERLY?
YES
NO
SEE FIGURE 6-17. BAND 3
UNIT OK

Figure 6-11. Main Troubleshooting Tree

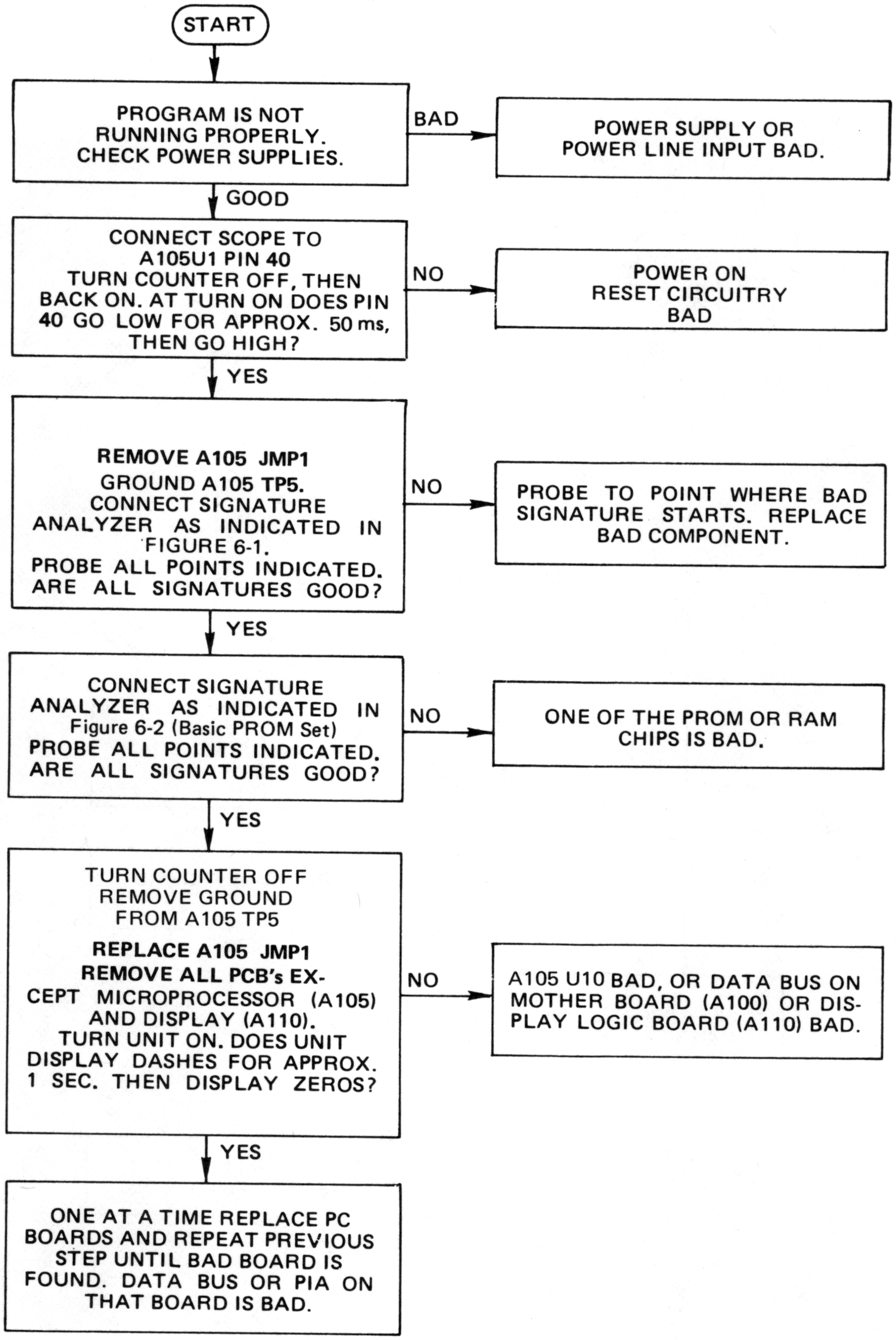

START
PROGRAM IS NOT RUNNING PROPERLY. CHECK POWER SUPPLIES.
BAD
POWER SUPPLY OR POWER LINE INPUT BAD.
GOOD
CONNECT SCOPE TO A105U1 PIN 40 TURN COUNTER OFF, THEN BACK ON. AT TURN ON DOES PIN 40 GO LOW FOR APPROX. 50 ms, THEN GO HIGH?
NO
POWER ON RESET CIRCUITRY BAD
YES
REMOVE A105 JMP1
GROUND A105 TP5. CONNECT SIGNATURE ANALYZER AS INDICATED IN FIGURE 6-1. PROBE ALL POINTS INDICATED. ARE ALL SIGNATURES GOOD?
NO
PROBE TO POINT WHERE BAD SIGNATURE STARTS. REPLACE BAD COMPONENT.
YES
CONNECT SIGNATURE ANALYZER AS INDICATED IN Figure 6-2 (Basic PROM Set) PROBE ALL POINTS INDICATED. ARE ALL SIGNATURES GOOD?
NO
ONE OF THE PROM OR RAM CHIPS IS BAD.
YES
TURN COUNTER OFF REMOVE GROUND FROM A105 TP5
REPLACE A105 JMP1 REMOVE ALL PCB's EXCEPT MICROPROCESSOR (A105) AND DISPLAY (A110). TURN UNIT ON. DOES UNIT DISPLAY DASHES FOR APPROX. 1 SEC. THEN DISPLAY ZEROS?
NO
A105 U10 BAD, OR DATA BUS ON MOTHER BOARD (A100) OR DISPLAY LOGIC BOARD (A110) BAD.
YES
ONE AT A TIME REPLACE PC BOARDS AND REPEAT PREVIOUS STEP UNTIL BAD BOARD IS FOUND. DATA BUS OR PIA ON THAT BOARD IS BAD.

Figure 6-12. Program Inoperative

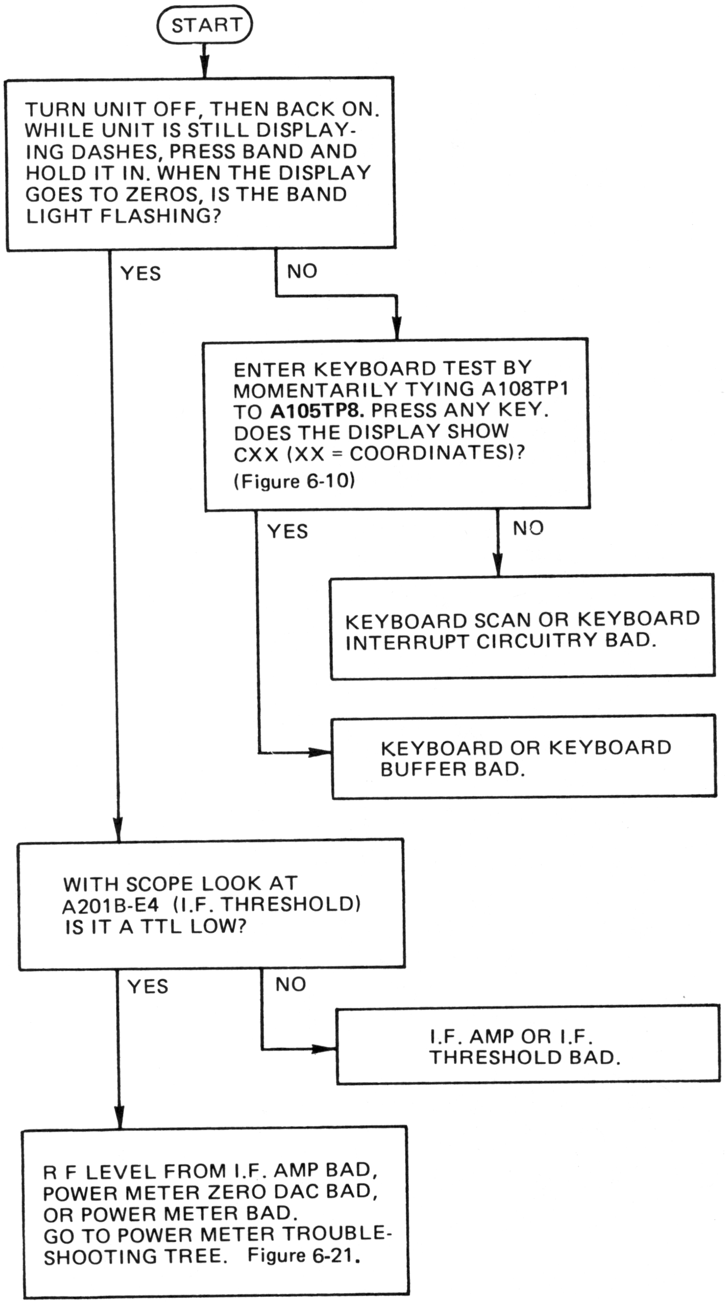

START
TURN UNIT OFF, THEN BACK ON. WHILE UNIT IS STILL DISPLAYING DASHES, PRESS BAND AND HOLD IT IN. WHEN THE DISPLAY GOES TO ZEROS, IS THE BAND LIGHT FLASHING?
YES
NO
ENTER KEYBOARD TEST BY MOMENTARILY TYING A108TP1 TO A105TP8. PRESS ANY KEY. DOES THE DISPLAY SHOW CXX (XX = COORDINATES)? (Figure 6-10)
YES
NO
KEYBOARD SCAN OR KEYBOARD INTERRUPT CIRCUITRY BAD.
KEYBOARD OR KEYBOARD BUFFER BAD.
WITH SCOPE LOOK AT A201B-E4 (I.F. THRESHOLD) IS IT A TTL LOW?
YES
NO
I.F. AMP OR I.F. THRESHOLD BAD.
R F LEVEL FROM I.F. AMP BAD, POWER METER ZERO DAC BAD, OR POWER METER BAD. GO TO POWER METER TROUBLESHOOTING TREE. Figure 6-21.

Figure 6-13. Keyboard

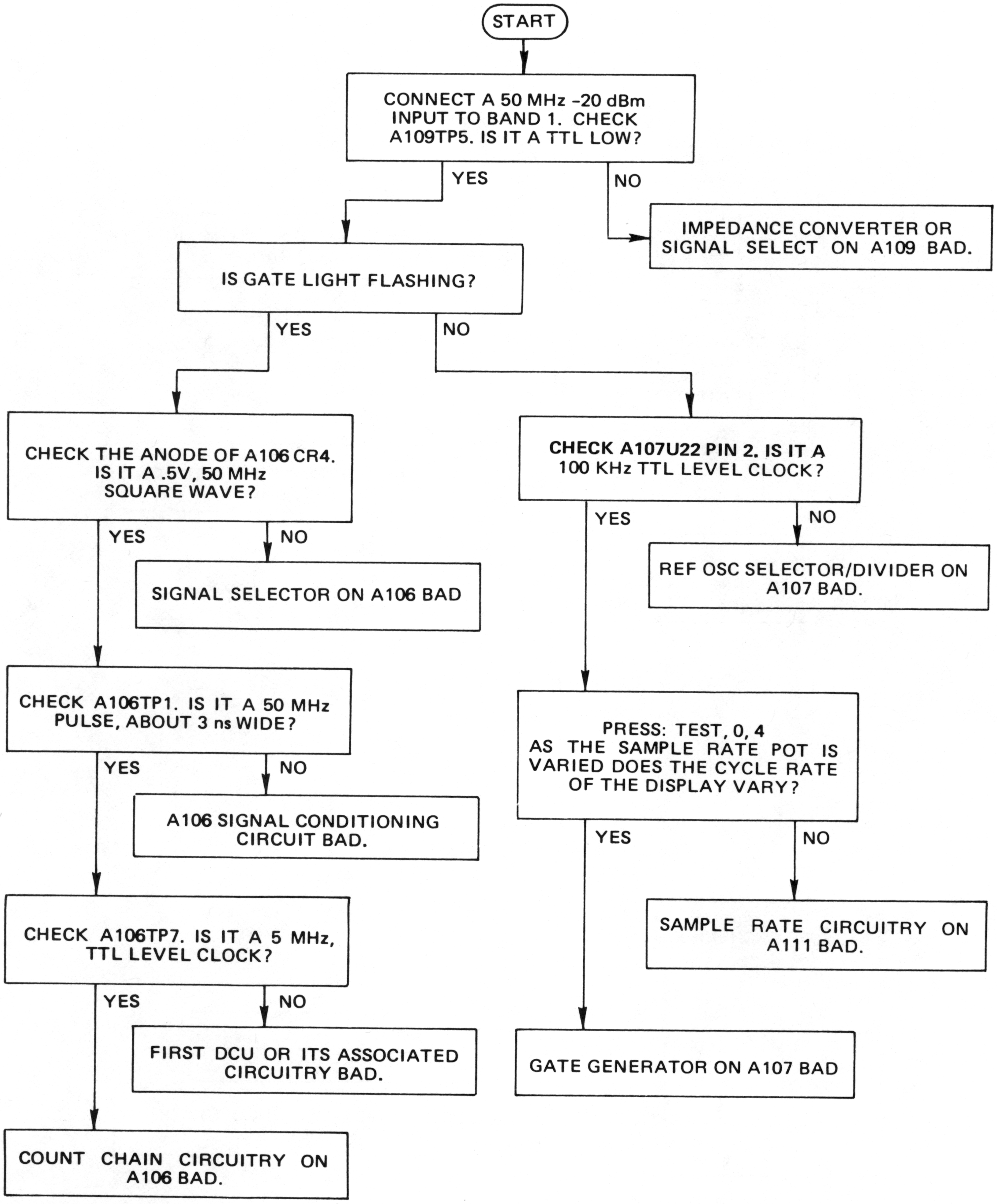

START
CONNECT A 50 MHz -20 dBm INPUT TO BAND 1. CHECK A109TP5. IS IT A TTL LOW?
YES
NO
IMPEDANCE CONVERTER OR SIGNAL SELECT ON A109 BAD.
IS GATE LIGHT FLASHING?
YES
NO
CHECK THE ANODE OF A106 CR4. IS IT A .5V, 50 MHz SQUARE WAVE?
YES
NO
SIGNAL SELECTOR ON A106 BAD
CHECK A106TP1. IS IT A 50 MHz PULSE, ABOUT 3 ns WIDE?
YES
NO
A106 SIGNAL CONDITIONING CIRCUIT BAD.
CHECK A106TP7. IS IT A 5 MHz, TTL LEVEL CLOCK?
YES
NO
FIRST DCU OR ITS ASSOCIATED CIRCUITRY BAD.
COUNT CHAIN CIRCUITRY ON A106 BAD.
CHECK A107U22 PIN 2. IS IT A 100 KHz TTL LEVEL CLOCK?
YES
NO
REF OSC SELECTOR/DIVIDER ON A107 BAD.
PRESS: TEST, 0, 4 AS THE SAMPLE RATE POT IS VARIED DOES THE CYCLE RATE OF THE DISPLAY VARY?
YES
NO
SAMPLE RATE CIRCUITRY ON A111 BAD.
GATE GENERATOR ON A107 BAD

Figure 6-14. Band 1

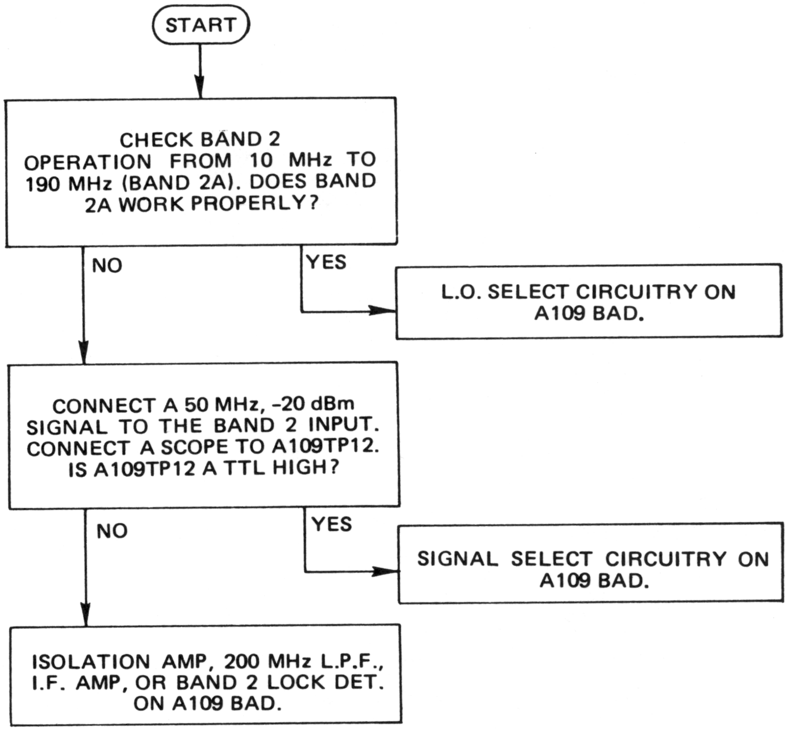

START
CHECK BAND 2 OPERATION FROM 10 MHz TO 190 MHz (BAND 2A). DOES BAND 2A WORK PROPERLY?
NO
YES
L.O. SELECT CIRCUITRY ON A109 BAD.
CONNECT A 50 MHz, -20 dBm SIGNAL TO THE BAND 2 INPUT. CONNECT A SCOPE TO A109TP12. IS A109TP12 A TTL HIGH?
NO
YES
SIGNAL SELECT CIRCUITRY ON A109 BAD.
ISOLATION AMP, 200 MHz L.P.F., I.F. AMP, OR BAND 2 LOCK DET. ON A109 BAD.

Figure 6-15. 200 MHz Test

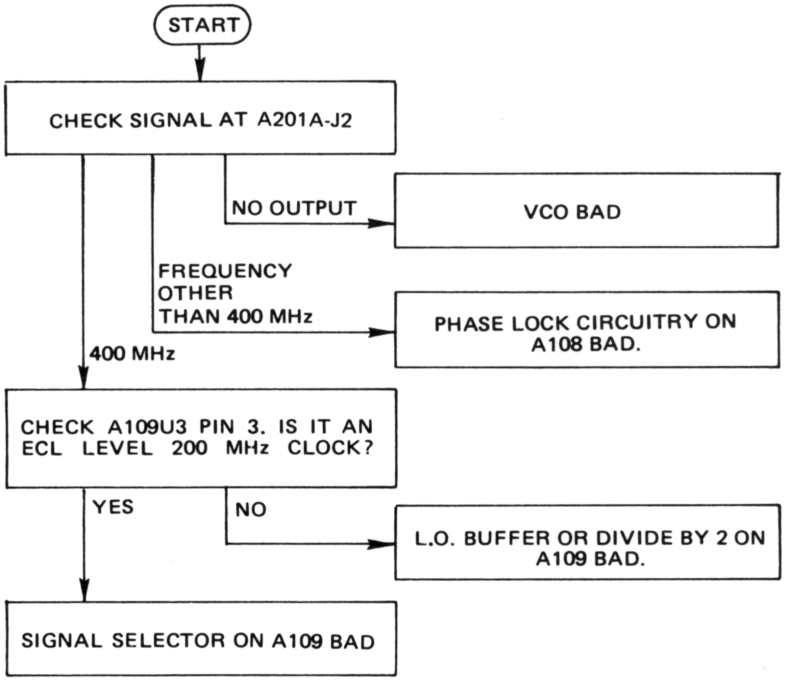
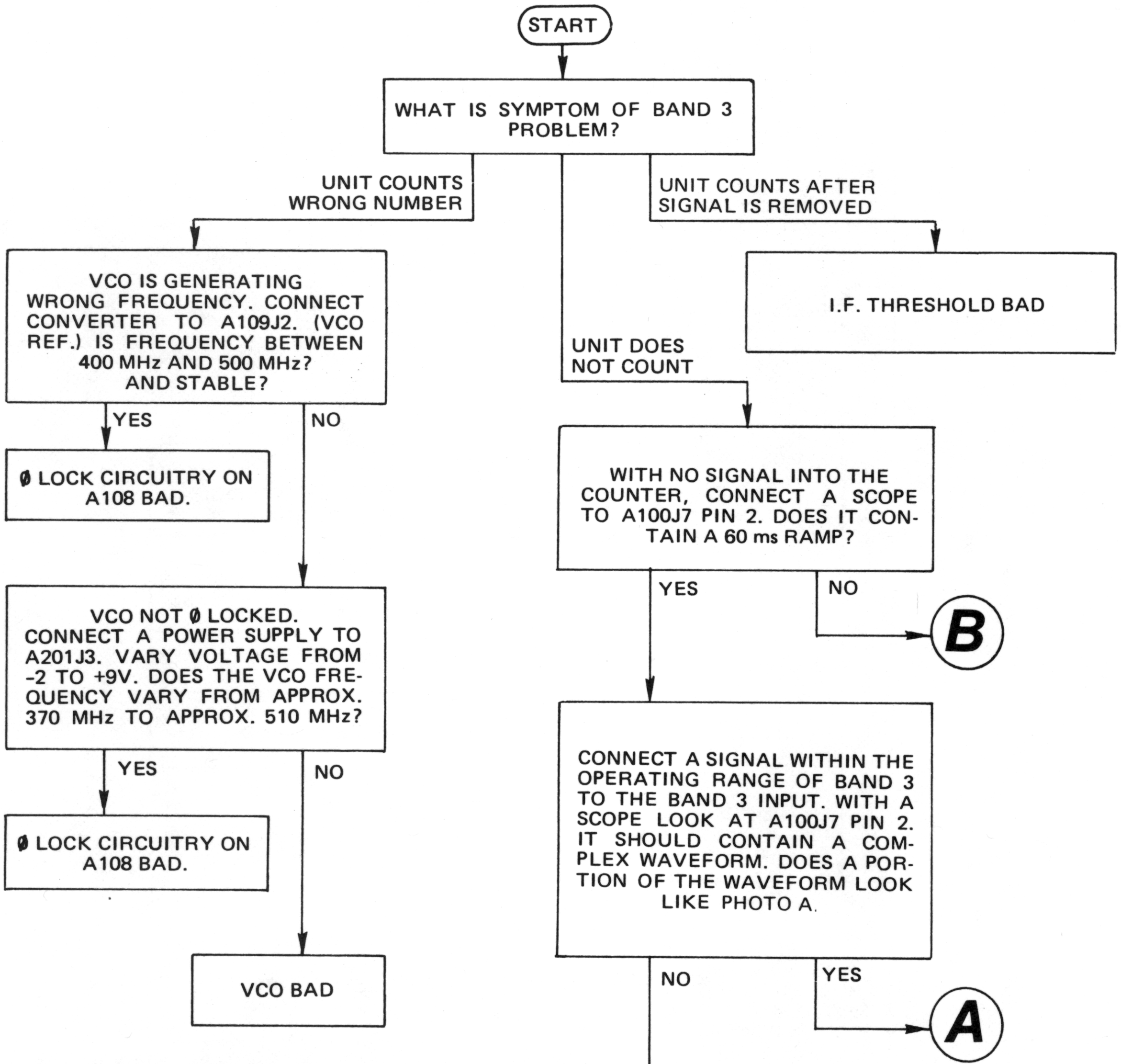

START
CHECK SIGNAL AT A201A-J2
NO OUTPUT
VCO BAD
FREQUENCY OTHER THAN 400 MHz
PHASE LOCK CIRCUITRY ON A108 BAD.
400 MHz
CHECK A109U3 PIN 3. IS IT AN ECL LEVEL 200 MHz CLOCK?
YES
NO
L.O. BUFFER OR DIVIDE BY 2 ON A109 BAD.
SIGNAL SELECTOR ON A109 BAD

Figure 6-16. Band 2


START
WHAT IS SYMPTOM OF BAND 3 PROBLEM?
UNIT COUNTS WRONG NUMBER
UNIT DOES NOT COUNT
UNIT COUNTS AFTER SIGNAL IS REMOVED
VCO IS GENERATING WRONG FREQUENCY. CONNECT CONVERTER TO A109J2. (VCO REF.) IS FREQUENCY BETWEEN 400 MHz AND 500 MHz? AND STABLE?
YES
NO
Ø LOCK CIRCUITRY ON A108 BAD.
VCO NOT Ø LOCKED. CONNECT A POWER SUPPLY TO A201J3. VARY VOLTAGE FROM -2 TO +9V. DOES THE VCO FREQUENCY VARY FROM APPROX. 370 MHz TO APPROX. 510 MHz?
YES
NO
Ø LOCK CIRCUITRY ON A108 BAD.
VCO BAD
I.F. THRESHOLD BAD
WITH NO SIGNAL INTO THE COUNTER, CONNECT A SCOPE TO A100J7 PIN 2. DOES IT CONTAIN A 60 ms RAMP?
YES
NO
B
CONNECT A SIGNAL WITHIN THE OPERATING RANGE OF BAND 3 TO THE BAND 3 INPUT. WITH A SCOPE LOOK AT A100J7 PIN 2. IT SHOULD CONTAIN A COMPLEX WAVEFORM. DOES A PORTION OF THE WAVEFORM LOOK LIKE PHOTO A.
NO
YES
A

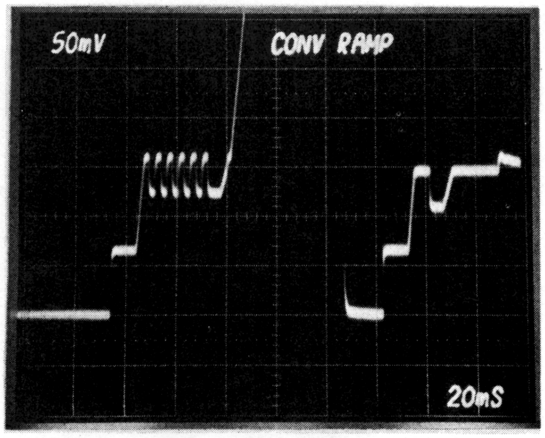


PHOTO A.

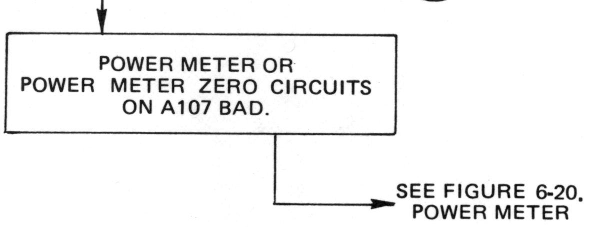

POWER METER OR POWER METER ZERO CIRCUITS ON A107 BAD.
SEE FIGURE 6-20, POWER METER

Figure 6-17. Band 3

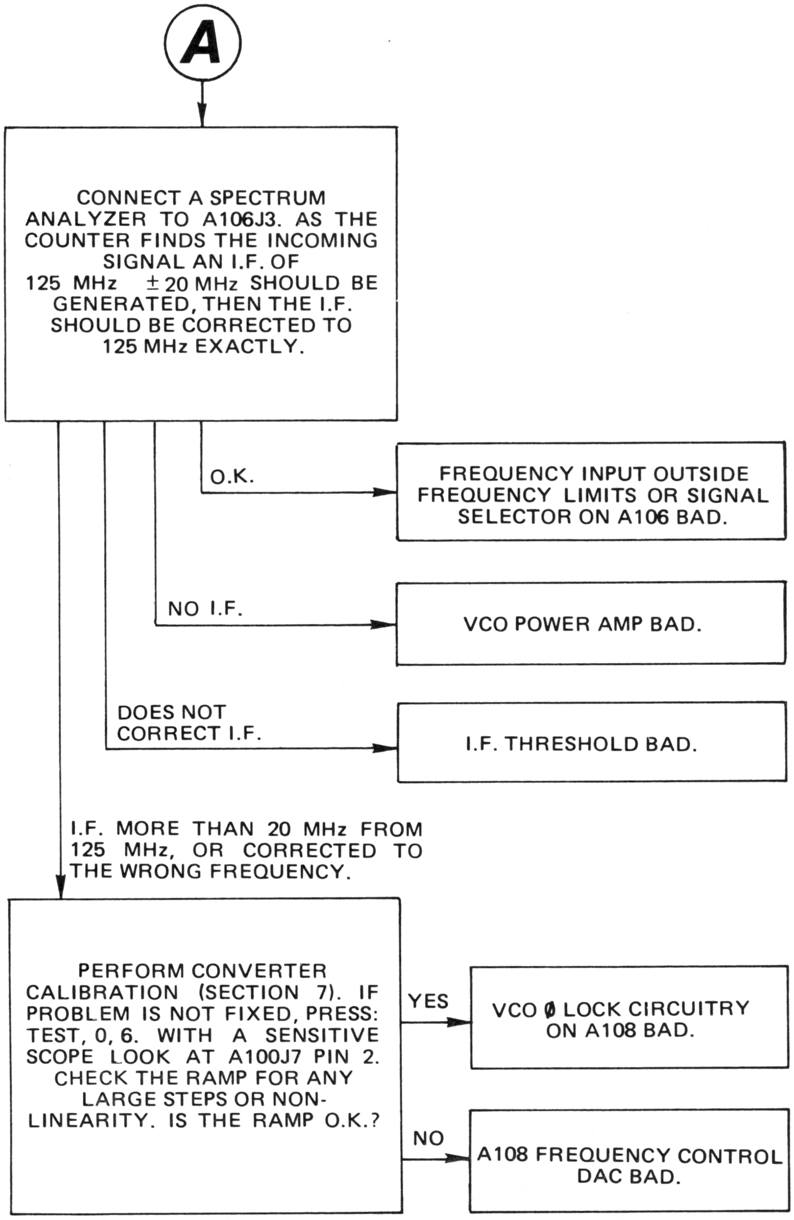

A
CONNECT A SPECTRUM ANALYZER TO A106J3. AS THE COUNTER FINDS THE INCOMING SIGNAL AN I.F. OF 125 MHz ±20 MHz SHOULD BE GENERATED, THEN THE I.F. SHOULD BE CORRECTED TO 125 MHz EXACTLY.
O.K.
FREQUENCY INPUT OUTSIDE FREQUENCY LIMITS OR SIGNAL SELECTOR ON A106 BAD.
NO I.F.
VCO POWER AMP BAD.
DOES NOT CORRECT I.F.
I.F. THRESHOLD BAD.
I.F. MORE THAN 20 MHz FROM 125 MHz, OR CORRECTED TO THE WRONG FREQUENCY.
PERFORM CONVERTER CALIBRATION (SECTION 7). IF PROBLEM IS NOT FIXED, PRESS: TEST, 0, 6. WITH A SENSITIVE SCOPE LOOK AT A100J7 PIN 2. CHECK THE RAMP FOR ANY LARGE STEPS OR NON-LINEARITY. IS THE RAMP O.K.?
YES
VCO φ LOCK CIRCUITRY ON A108 BAD.
NO
A108 FREQUENCY CONTROL DAC BAD.

Figure 6-17. Band 3, continued

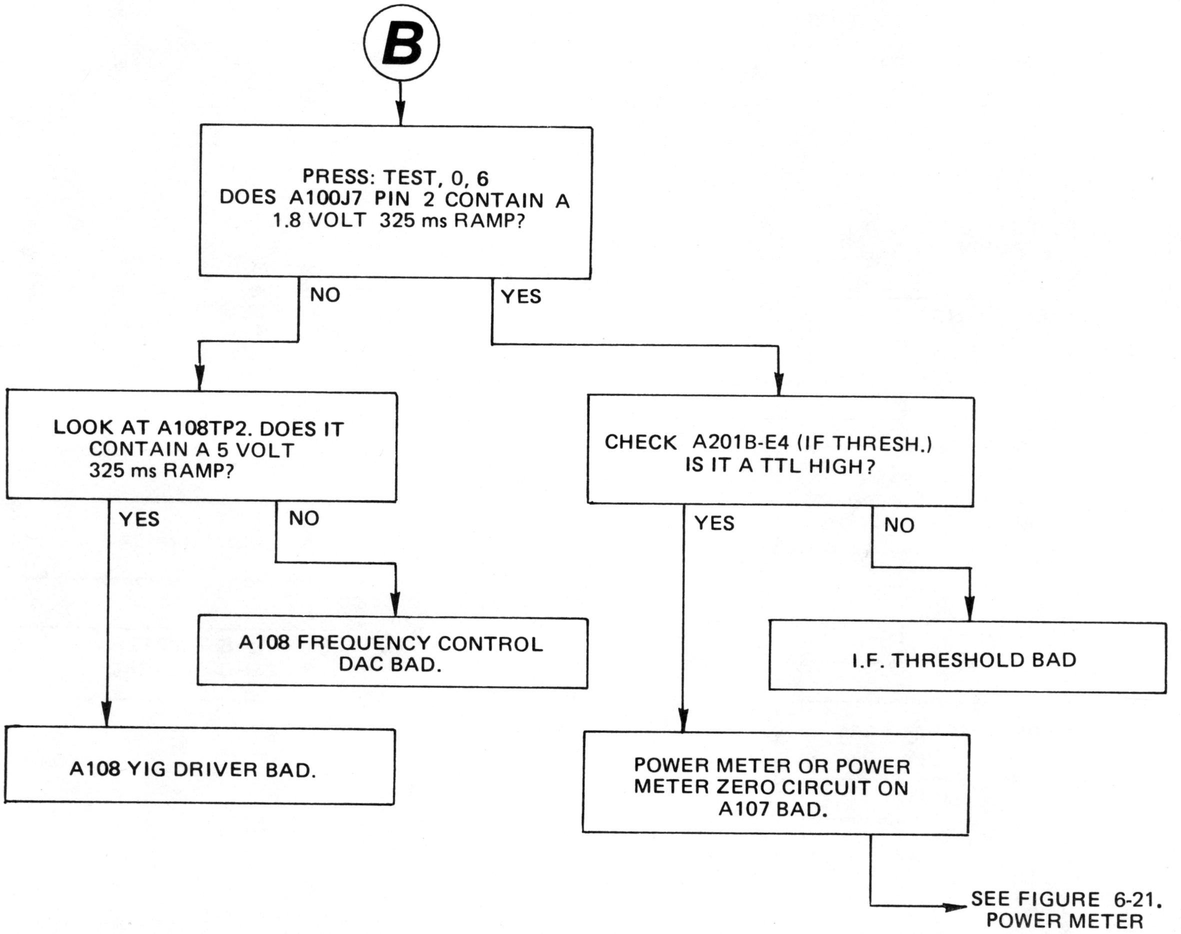

B
PRESS: TEST, 0, 6
DOES A100J7 PIN 2 CONTAIN A 1.8 VOLT 325 ms RAMP?
NO
YES
LOOK AT A108TP2. DOES IT CONTAIN A 5 VOLT 325 ms RAMP?
CHECK A201B-E4 (IF THRESH.) IS IT A TTL HIGH?
YES
NO
YES
NO
A108 FREQUENCY CONTROL DAC BAD.
I.F. THRESHOLD BAD
A108 YIG DRIVER BAD.
POWER METER OR POWER METER ZERO CIRCUIT ON A107 BAD.
SEE FIGURE 6-21. POWER METER

Figure 6-17. Band 3, continued

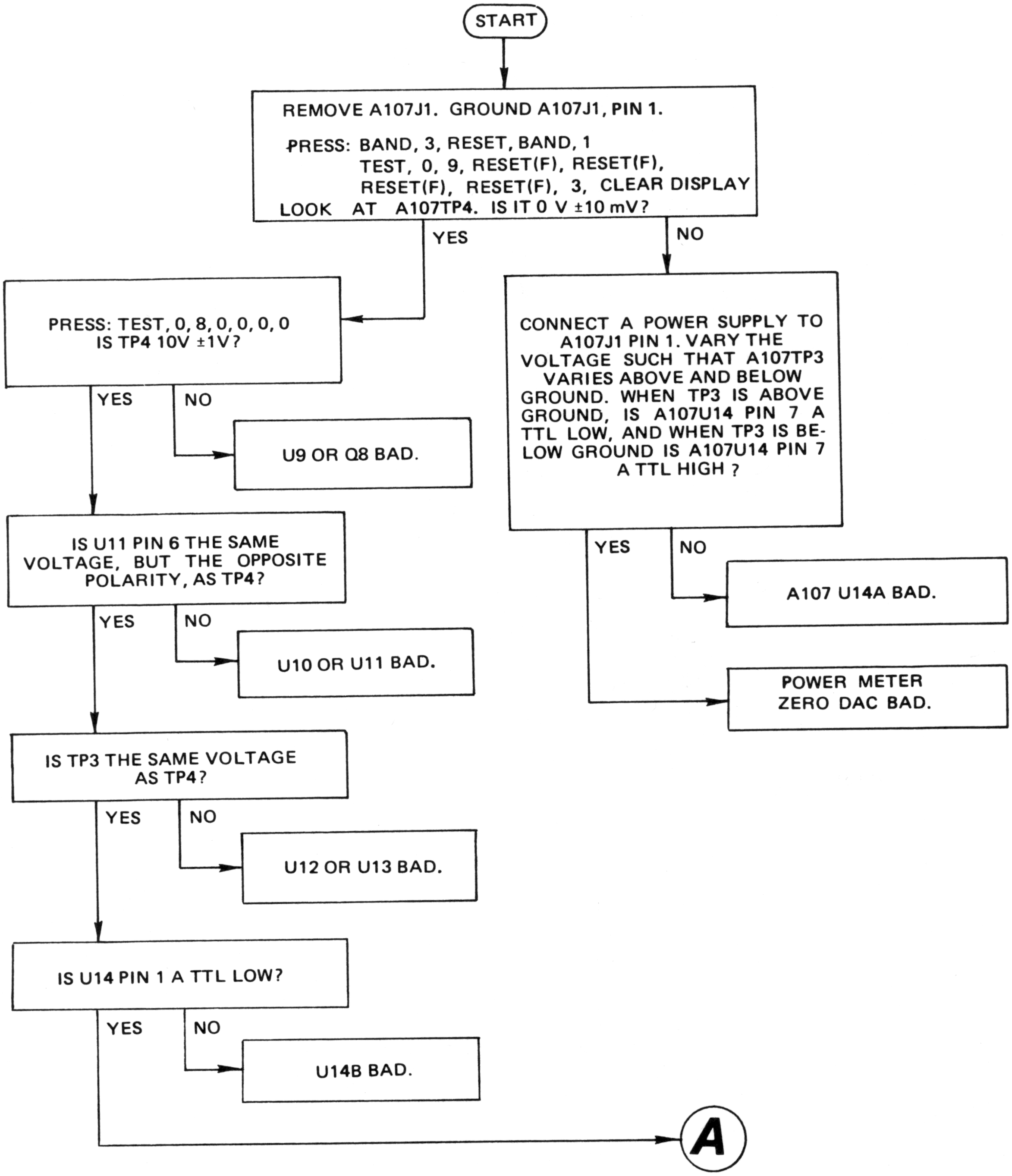

START
REMOVE A107J1. GROUND A107J1, PIN 1.
PRESS: BAND, 3, RESET, BAND, 1
TEST, 0, 9, RESET(F), RESET(F),
RESET(F), RESET(F), 3, CLEAR DISPLAY
LOOK AT A107TP4. IS IT 0 V ±10 mV?
YES
NO
PRESS: TEST, 0, 8, 0, 0, 0, 0
IS TP4 10V ±1V?
YES
NO
U9 OR Q8 BAD.
IS U11 PIN 6 THE SAME VOLTAGE, BUT THE OPPOSITE POLARITY, AS TP4?
YES
NO
U10 OR U11 BAD.
IS TP3 THE SAME VOLTAGE AS TP4?
YES
NO
U12 OR U13 BAD.
IS U14 PIN 1 A TTL LOW?
YES
NO
U14B BAD.
A
CONNECT A POWER SUPPLY TO A107J1 PIN 1. VARY THE VOLTAGE SUCH THAT A107TP3 VARIES ABOVE AND BELOW GROUND. WHEN TP3 IS ABOVE GROUND, IS A107U14 PIN 7 A TTL LOW, AND WHEN TP3 IS BELOW GROUND IS A107U14 PIN 7 A TTL HIGH ?
YES
NO
A107 U14A BAD.
POWER METER ZERO DAC BAD.

Figure 6-18. Power Meter and Power Meter Zero DAC

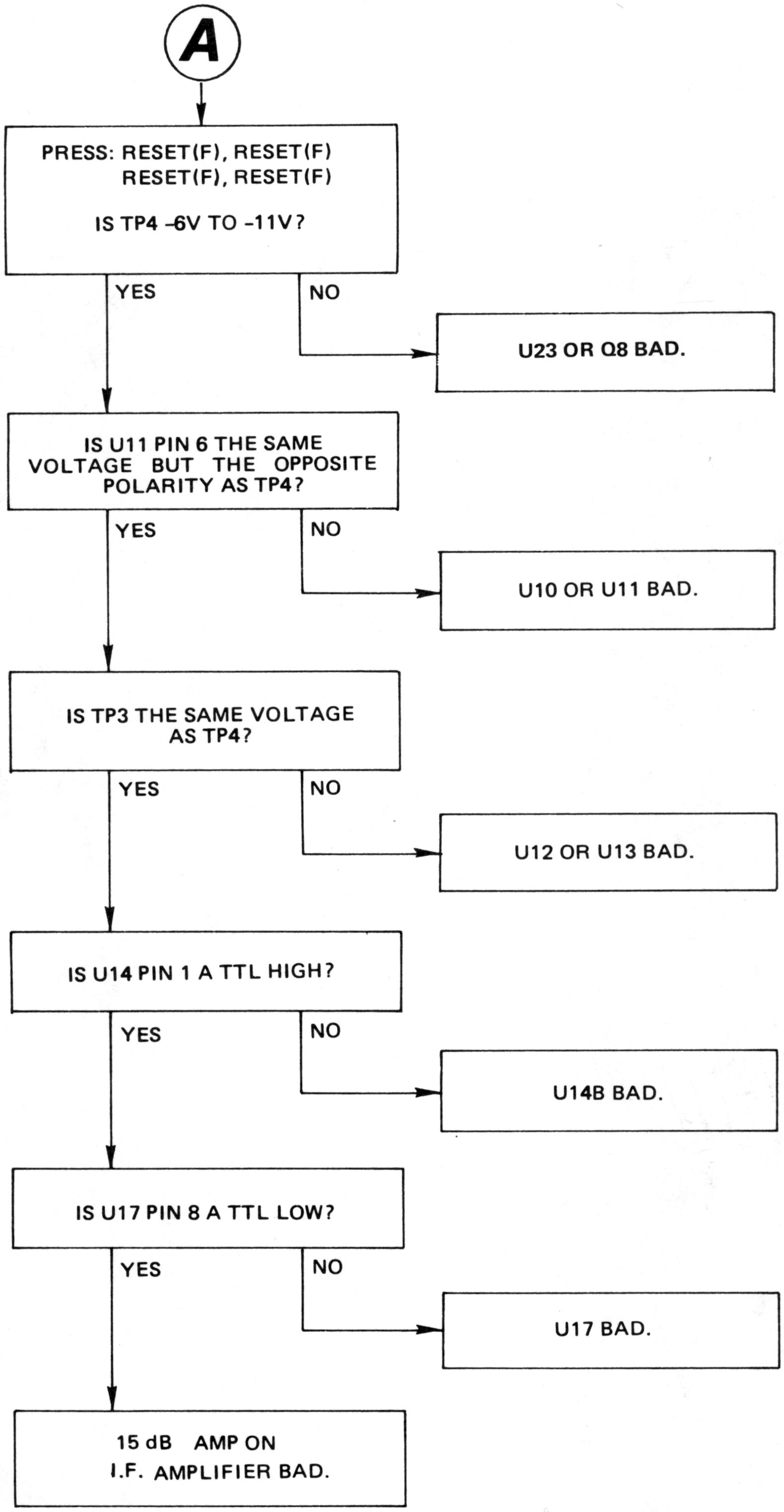

A
PRESS: RESET(F), RESET(F)
RESET(F), RESET(F)
IS TP4 -6V TO -11V?
YES
NO
U23 OR Q8 BAD.
IS U11 PIN 6 THE SAME VOLTAGE BUT THE OPPOSITE POLARITY AS TP4?
YES
NO
U10 OR U11 BAD.
IS TP3 THE SAME VOLTAGE AS TP4?
YES
NO
U12 OR U13 BAD.
IS U14 PIN 1 A TTL HIGH?
YES
NO
U14B BAD.
IS U17 PIN 8 A TTL LOW?
YES
NO
U17 BAD.
15 dB AMP ON
I.F. AMPLIFIER BAD.

Figure 6-18. Power Meter and Power Meter Zero DAC, continued

Section 7
Adjustments and Calibrations

GENERAL

To correctly adjust the 545A or 548A counter use the following procedures. Adjustments should only be made if the counter does not operate as specified, or following the replacement of components. If the adjustments do not result in the performance specified then refer to the troubleshooting section of this manual. The test equipment required is:

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
Tektronix	475	Oscilloscope	General Purpose
Fluke	8050A	D.V.M.	4½ digit resolution
H.P.	182C, 8559A	Spectrum Analyzer	125 MHz
Wavetek	2002	Sweeper	10 MHz - 2 GHz
Wiltron	610D, 6237D	Microwave Sweeper	2 GHz - 18 GHz
H.P.	8690A, 8696A	Microwave Sweeper	18 GHz - 26.5 GHz
EIP	2000017	Service Kit	See Appendix A (A-3)

POWER SUPPLY ADJUSTMENTS

Prior to making any adjustments to the power supply the counter should "warm up" at least 20 minutes.

Voltages are measured on the back of the Interconnect board (A100), or on the back of the Power Supply board (A101).

1. Connect the Digital Volt Meter (DVM) between ground and +12V.
2. Adjust A101 R5 until the voltage measures +12.000 VDC ± .010 VDC.
3. Connect the DVM between ground and -12 V.
4. Adjust A101 R17 until the voltage measures -12.000 VDC ± .010 VDC.

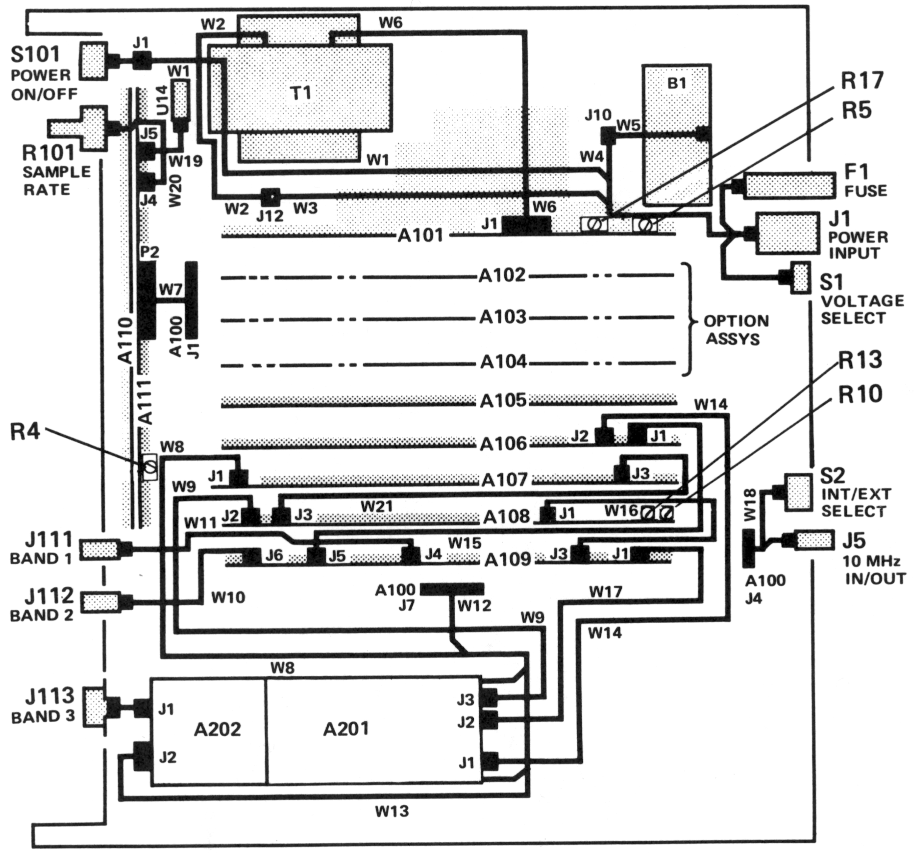

W2
W6
S101
POWER
ON/OFF
J1
W1
U14
T1
B1
R17
R5
R101
SAMPLE
RATE
J5
W19
W20
J4
J10
W5
W1
W4
W2
J12
W3
J1
W6
A101
F1
FUSE
J1
POWER
INPUT
S1
VOLTAGE
SELECT
P2
W7
A110
A100
J1
A102
A103
A104
OPTION
ASSYS
R13
R10
A111
A105
W14
R4
W8
A106
J2
J1
W9
J1
A107
J3
S2
INT/EXT
SELECT
W18
J2
J3
W21
A108
J1
W16
W11
J111
BAND 1
J6
J5
J4
W15
A109
J3
J1
J5
10 MHz
IN/OUT
A100
J4
J112
BAND 2
W10
A100
J7
W12
W17
W9
W14
W8
J113
BAND 3
J1
A202
A201
J3
J2
J2
J1
W13

Figure 7-1. Adjustment Locations.

CONVERTER CALIBRATION

COARSE ADJUSTMENT

1. Press: BAND 3, TEST 1 0,
9 8 4 2 0 3
9 8 4 0 ± (E) 8

2. Set the microwave sweeper at 2.00 GHz ± 10 MHz, about -10 dBm.

3. Connect the sweeper output to band 3 of the counter.

4. Connect the oscilloscope to A201B-E5 (RF level).

5. Adjust A108R13 until A201B-E5 is at maximum positive voltage.

6. Set the sweeper to 15.00 GHz ± 10 MHz.

7. On the counter press: 9 8 4 2 1 • (D)
9 8 4 0 4 CLEAR DATA (C)

8. Adjust A108R10 until A201B-E5 is at maximum negative voltage.

9. Set the sweeper to 2.00 GHz ± 10 MHz.

10. On the counter press: 9 8 4 2 0 3
9 8 4 0 ± (E) 8

11. Adjust A108R13 until A201B-E5 is at maximum negative voltage.

12. On the counter press: CLEAR DISPLAY

FINE ADJUSTMENT

1. Set the sweeper to 1.0 GHz ± 10 MHz.

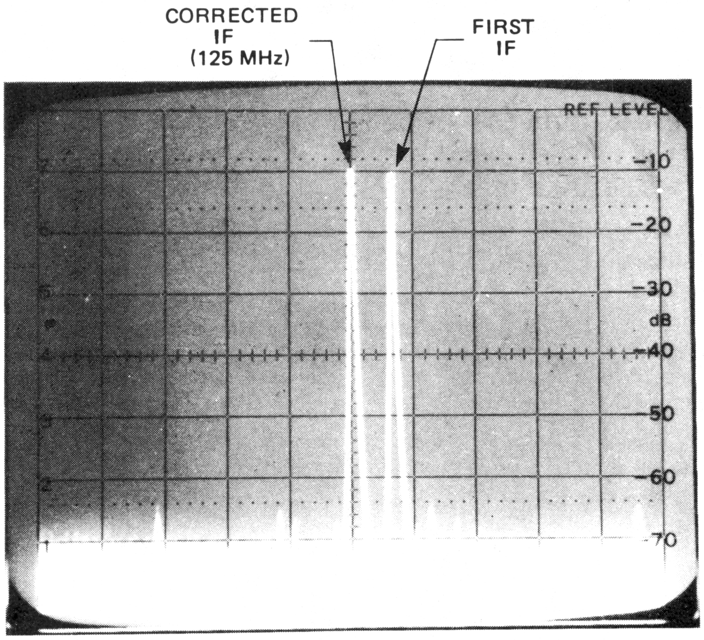
2. Connect the spectrum analyzer to A106J4 (IF output).

3. The counter should be counting the incoming signal. The spectrum analyzer should be displaying the IF (125 MHz).

4. On the counter press RESET ☐. When the converter finds the incoming signal an IF is generated which is near 125 MHz at first, then shifts to exactly 125 MHz (see figure 7-2). If the first IF is more than 5 MHz from 125 MHz, adjust A108R14 until the first IF (at an input frequency of 1 GHz) is 125 MHz ± 5 MHz.

5. Slowly tune the microwave sweeper from 1 to 26.5 GHz (to 18 GHz for 545), while pressing RESET ☐ on the counter.

6. Every time the converter finds the incoming signal the first IF should be 125 MHz ± 20 MHz. If not, adjust A108R10 until the first IF is always 125 MHz ± 20MHz.



CENTER FREQUENCY: 125 MHz

SCAN WIDTH: 5 MHz/div

Figure 7-2. If Signal.

TIME BASE CALIBRATION

It is important to note that the precision of the time base calibration directly affects overall counter accuracy. Reasons for recalibration, and the procedures to be used, should be thoroughly understood before attempting any readjustment.

The fractional error in the frequency indicated by the counter, is equal to the negative of the fractional frequency error of the Time Base Oscillator with respect to its true value. That is:

$$\frac{\triangle f_s}{f_s} = \frac{\triangle f_t}{f_t}$$

where f_s is the true frequency of the measured signal, and f_t is the true frequency of the Time Base Oscillator. Thus, the inaccuracy associated with a frequency measurement is directly related to the quality of the Time Base Oscillator, and a measure of the precision with which it was originally adjusted.

TEMPERATURE COMPENSATED CRYSTAL OSCILLATOR (TCXO)

The standard Time Base Oscillator used in the counter is a TCXO (A116). The range of the actual measured frequencies of this oscillator will differ by no more than 2 parts in 10^6 if the temperature is slowly varied from 0 to +50 degrees C.

With a stable input frequency, the measurement indicated by the counter will fluctuate proportionally to the TCXO drift. To center this fluctuation on the true value of the measured signal, each TCXO has imprinted on its side the frequency setting required at +25 degrees C.

At approximate room temperature (+25 degrees C.), the slope of the frequency vs. temperature curve is normally no worse than $\pm 1 \times 10^{-7}$ parts per degree C. When the counter is used in an ordinary laboratory environment, the TCXO may be set as close to 10,000,000 Hz as desired. In this environment, a peak-to-peak temperature variation of 5° C. will result in a measured signal error of no more than $\pm\ 2.5 \times 10^{-7}$ parts. This signal error is due to the temperature characteristics of the Time Base Oscillator.

The natural aging characteristics of the crystal in the Time Base Oscillator can also cause inaccurate signal measurements. Aging refers to the long term, irreversible change in frequency (generally in the positive direction) which all quartz oscillators experience. The magnitude of this frequency fluctuation in the TCXO is less than 3×10^{-7} parts per month as specified. This may improve to at least 1×10^{-6} parts per year when in continuous operation.

Error due to aging adds directly to error due to temperature. The number of times the counter requires recalibration depends on the environment in which the counter operates, and upon the level of accuracy required.

For example, if the counter is subjected to the full operating temperature range one month after proper initial adjustments, the inaccuracy could vary from $+1.3 \times 10^{-6}$ parts to -0.7×10^{-6} parts.

TCXO CALIBRATION PROCEDURES

METHOD 1 (with accurate frequency counter)

1. Remove top cover of counter. Connect counter to reliable power source. Note ambient temperature.

2. Measure the frequency of the TCXO (at the rear panel 10 MHz connector) with a second counter of known calibration accuracy.

3. Adjust the TCXO by turning the calibration screw on the TCXO case until the measured frequency equals that shown on the TCXO calibration label.

METHOD 2 (with accurate frequency source)

1. Apply a 10 000 000 Hz signal from a frequency standard (or other oscillator of suitable accuracy and stability) to the Band 1 input of the counter.

2. Press RESOL ☐ [0] (1 Hz resolution)

3. Adjust the TCXO until the reading on the counter is offset from 10 000 000 Hz by the negative of the frequency shown on the TCXO. For example, if the TCXO calibration label shows a frequency of 10 000 003 Hz, adjust the TCXO until the counter displays 9 999 997 Hz.

DISPLAY INTENSITY

On the front panel logic assembly (A111) R4 may be adjusted to provide the most comfortable display intensity.

Section 8
Performance Tests

GENERAL

These tests are for the basic counter. Peformance tests for options are in section 10. These tests will enable the user to verify that the counter is operating within specifications.

VARIABLE LINE VOLTAGE

During the performance tests the counter should be connected to the power source, through a variable voltage device, so that line voltage may be varied ±10% from nominal. This will assure proper operating of the counter under various supply conditions.

REQUIRED TEST EQUIPMENT
(or equivalent)

MANUFACTURER	MODEL	DESCRIPTION	CRITICAL PARAMETERS
H.P.	651B	Signal Generator	10 Hz - 10 MHz
Wavetek	2002	Sweeper	10 MHz - 2 GHz
Wiltron	610D, 6237D	Microwave Sweeper	2 GHz - 18 GHz
H.P.	8690A, 8696A	Microwave Sweeper	18 GHz - 26.5 GHz

BAND 1
(10 Hz - 100 MHz)

1. Set the counter to band 1.
2. Connect the signal source output, through a 50 ohm shunt feedthrough resistor, to the band 1 input on the counter.
3. Set the signal level to 25 mv RMS (-19 dBm into 50 ohms).
4. Vary the signal from 10 Hz to 100 MHz (changing signal source as required).

The counter should display the correct input frequency.

BAND 2
(10 MHz - 1 GHz)

1. Set the counter to band 2.

2. Connect the signal source output to the band 2 input of the counter.

3. Set the signal level to -20 dBm (22 mv RMS).

4. Vary the signal input from 10 MHz to 1 GHz.

The counter should display the correct input frequency.

BAND 3
(548A: 1 GHz - 26.5 GHz)
(545A: 1 GHz - 18 GHz)

1. Set the counter to band 3.

2. Connect the signal source output to the band 3 input of the counter.

3. Vary the signal frequency from 1 GHz to 18/26.5 GHz (changing the signal source as required) at the following levels.

1 GHz – 12.4 GHz	-30 dBm (7 mv RMS)
12.4 GHz – 18 GHz	-25 dBm (12 mv RMS)
18 GHz – 22 GHz	-20 dBm (22 mv RMS)
22 GHz –26.5 GHz	-15 dBm (38 mv RMS)

The counter should display the correct input frequency.

Section 9
Functional Description and Illustrated Parts Breakdown

This section contains a functional description, a parts list, an illustration and a schematic diagram for each printed circuit board used in this counter.

The parts list is broken down by types of components, listed in alphanumeric sequence. The components that have a different reference designator (REF DES), but have the same EIP part number, are described for the first such component listed. Subsequent descriptions of that component will refer to the first entry. The total number of like components used on the same assembly will be listed with the first entry in the column identified as UNITS PER ASSY.

The last two columns of the parts list wil supply the name of the manufacturer and their Federal Supply Code for manufacturers (FSCM) number. A list of manufacturers names, addresses and their Federal Supply Code for Manufacturers (FSCM) number are given in Appendix A. The FSCM number is used in the parts list as a guide to the manufacturer or supplier of a part.

Pages 9-3 through 9-5 contain the top assembly of the counter and other basic information. After page 9-5 you will note that the page numbers have a three digit first number followed by a dashed number. The three digit number reflects the number of the assembly being described on those pages. The dashed number is the page sequence for the description of that assembly. For example, pages 105-1 through 105-5 all relate to the A105 printed circuit board. This page numbering system facilitates simple, modular page replacement when an assembly revision makes a manual update necessary.

REFERENCE DESIGNATORS

A	Assembly
B	Battery or Fan
C	Capacitor
CR	Diode
DS	Indicator (display)
F	Fuse
J	Jack or Connector
K	Relay
L	Inductor
P	Plug or PCB contacts
Q	Transistor
R	Resistor
S	Switch
T	Transformer
TP	Test Point
U	Integrated Circuit
X	Socket or Holder
Q1-3	Q1 *through* Q3
Q1/2	Q1 *and* Q2 (matched pair)

ABBREVIATIONS

CBN	Carbon
CER	Ceramic
CMT	Cermet
CNTR	Counter
CONV	Converter
COMP	Composition
CONN	Connector
ELEC	Electrolytic
FDTH	Feedthrough
FLM	Film
FML	Female
GP	General Purpose
IC	Integrated Circuit
K	Kilo (x 1,000)
LED	Light-emitting-diode
M	Meg (x 1,000,000)
MET OX	Metal Oxide
mF	Metal Film
mH	Millihenry
ML	Male

MTCH PR	Matched Pair
PC	Printed Circuit
PCB	PC Board Assembly
pF	Picofarad
PREC	Precision
RSTR	Resistor
RT AN	Right Angle
S.A.T.	Value or type selected during factory test. Part may not be used.
SW	Switch
TANT	Tantalum
TRIM	Trimmer
uF	Microfarad
uH	Microhenry
VAR	Variable
WPRF	Waterproof
WW	Wirewound
XSTR	Transistor

545A/548A MICROWAVE COUNTER

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
	COUNTER, MODEL 545A	2000022		EIP	
	MODEL 548A	2000023		EIP	
-1	FRONT PANEL ASSY	2010218	1		
	Knob	5210223	1	5000160	31013
	Button set, 12 + 9	5210220	1	5230005-02	
	Panel	5210378	1		
	Sample Rate Control Assy	2010134	1		
	Alignment Pin	5210190	2		
	Retainer Key	5210191	1		
	Switch, toggle, PWR	2010187	1		
-2	REAR PANEL ASSY	2010219	1		
	Panel	5210192	1		
	Conn, Filter	2650005	1	3EF1	05245
	Switch, toggle, SPDT, 120V, 5A	4510001	1	7101H	09353
	Fuse holder	5000172	1	031.1653/1666/1663	
	Fuse, 1A, SB, 250V	5000085	1	MDL -1A	71400
	Fuse, .50A, SB	5000169	1	FST034-3114	71400
	Conn, BNC	2610024	1	KC -79 -35	91836
	Voltage Select Switch Assy, A151	2010159	1		
-3	FAN ASSY	2010136	1		
	Fan	5000151	1	760/126LF/182/1115	
	Conn, Plug, 3 pin	2620110	1	03 - 06 - 2032	0000A
	Contact, Male	2620038	2	02 - 06 - 2103	0000A
	Spacer	5210016	2		
-4	FRAME KIT	2010151	1		
	Panel, Side, Enclosure	5210210	2		
	Trim, Front Post	5220004	2		
	Trim, Handle	5220025	2		
	Frame	5210248	2		
	Corner Post, Front	5250001	2		
	Corner Post, Rear	5250002	2		
	Handle, Enclosures	5250011	2		
-5	TRANSFORMER, ASSY, A1T1	2010155	1		
	Transformer, Power	4900005	1		
	Conn, Plug, 9 pin	2620112	1	03 - 06 - 2092	0000A
	Conn, Housing, 6 pin	2620129	Ref	640427 - 6	AMP
	Contact, Male	2620038	7	02 - 06 - 2103	0000A
	Contact, Female	2620036		02 - 06 - 1103	0000A
-6	FRONT CARD GUIDE ASSY	2010156	1	5210199	
-7	REAR CARD GUIDE ASSY	2010157	1		
-8	TOP COVER ASSY	2010212	1		
-9	BOTTOM COVER	5210209	1		
-10	TILT BAIL	5000055	1		
-11	Foot, Plastic Enclosure	5220003	4		
-12	Line Cord Set - Domestic	5440002	1		
	Line Cord Set - Export	5440017	1		

545A/548A MICROWAVE COUNTER continued

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
	PCB ASSEMBLIES			See Page No.	
A100	Counter Interconnect	2020180	1	100 - 1	
A101	Power Supply	2020131	1	101 - 1	
A105	Microprocessor	2020195	1	105 - 1	
A106	Count Chain	2020136	1	106 - 1	
A107	Gate Generator	2020197	1	107 - 1	
A108	Converter Control (Band 3)	2020198	1	108 - 1	
A109	Band 2 Converter	2020139	1	109 - 1	
A110	Display and Keyboard Logic	2020140	1	110 - 1	
A111	Front Panel Logic	2020191	1	111 - 1	
A203	Microwave Converter	2010142	1	200 - 1	
A201A	Voltage Control Oscillator	2020142	1	201 - 1	
A201B	IF Amplifier	2020143	1	202 - 1	
A202	Microwave (YIG) not shown				
	CABLES:				
W7	Front Panel, Flat Ribbon	2040169	1		
W19, 20	Front Panel, Harness	2040168	1		
W1, 3, 5	Rear Panel, Harness	2040167	1		
W10	(A1J111-A109J6) Band 1, Coax	2040165	1		
W11	(A112-A109J4) Band 2, Coax	2040166	1		
W16	(A108J1-A09J3), Coax	2040208	1		
W15	(A106J2-A109J5), Coax	2040210	1		
W12, 13	VCO/IF, Harness	2040170	1		
W14	(A201BJ1-A106J2), Coax	2040172	1		
W8	(A201J4-A107J1), Coax	2040173	1		
W9	(A201AJ3-A108J2), Coax	2040174	1		
W17	(A201AJ3-A109J1), Coax	2040175	1		
	PROMS:				
A105 –	BASIC PROM SET				
U15	Section 1	6500002-01			
U17	Section 2	6500002-02			
U13	Section 3	6500002-03			
A105 –	GPIB OPTION				
U16		6400002-02		**–FOR REFERENCE ONLY**	
A107 –	POWER METER OPTION			**SEE PARTS LIST OF EACH ASSEMBLY OR OPTION FOR PROM DESCRIPTION**	
U20		6400002-04			
A105 –	BAND 4 OPTION				
U14		6400002-01			
A105 –	BCD REMOTE PROGRAMMING OPTION				
U16		6400002-03			

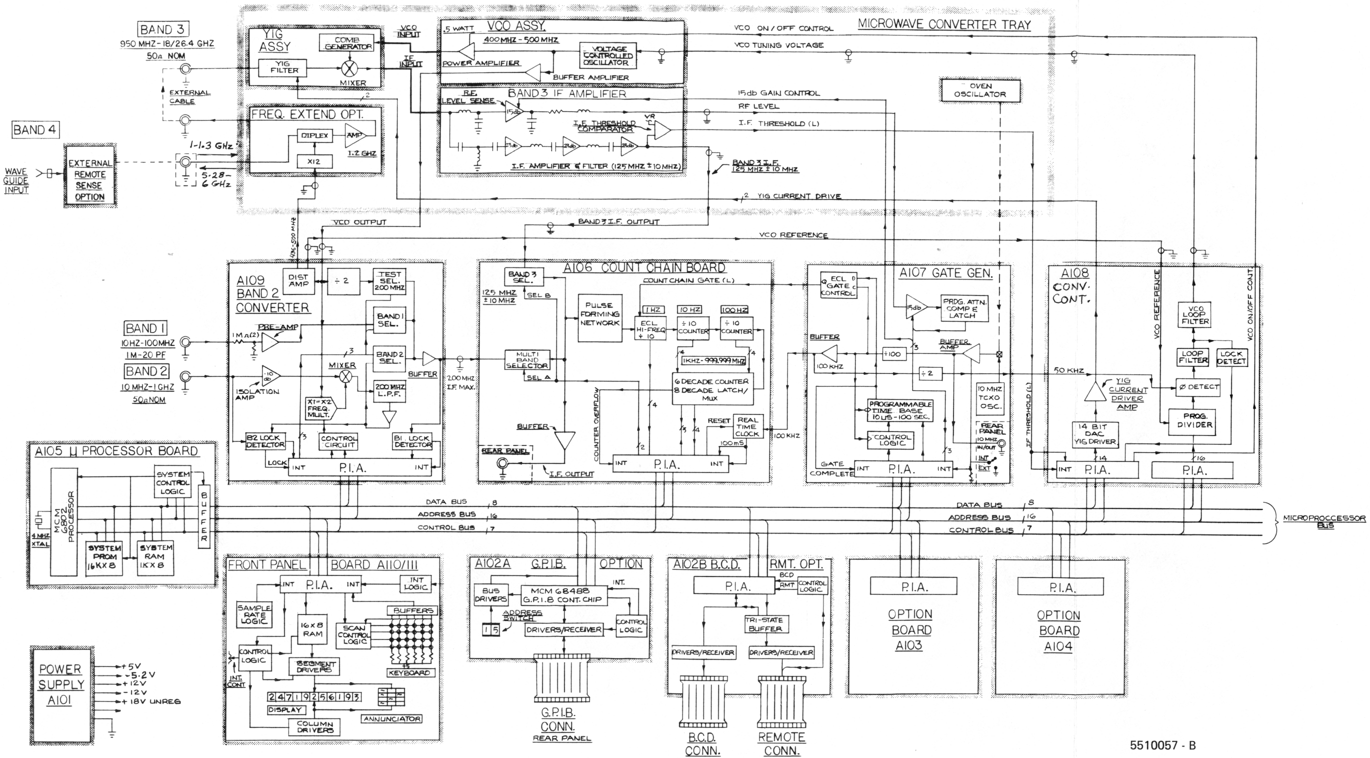

MICROWAVE CONVERTER TRAY
BAND 3
950 MHZ - 18/26.4 GHZ
50Ω NOM
BAND 4
WAVE GUIDE INPUT
EXTERNAL REMOTE SENSE OPTION
EXTERNAL CABLE
1-1.3 GHz
5.28-6 GHz
YIG ASSY
YIG FILTER
COMB GENERATOR
MIXER
FREQ. EXTEND OPT.
DIPLEX
AMP
X12
1.2 GHZ
VCO INPUT
I.F. INPUT
VCO ASSY.
.5 WATT
400 MHZ - 500 MHZ
POWER AMPLIFIER
VOLTAGE CONTROLLED OSCILLATOR
BUFFER AMPLIFIER
BAND 3 IF AMPLIFIER
R.F. LEVEL SENSE
I.F. THRESHOLD COMPARATOR
I.F. AMPLIFIER & FILTER (125 MHZ ± 10 MHZ)
BAND 3 I.F. 125 MHZ ± 10 MHZ
VCO ON / OFF CONTROL
VCO TUNING VOLTAGE
15db GAIN CONTROL
RF LEVEL
I.F. THRESHOLD (L)
OVEN OSCILLATOR
YIG CURRENT DRIVE
VCO OUTPUT
BAND 3 I.F. OUTPUT
VCO REFERENCE
A109 BAND 2 CONVERTER
DIST AMP
÷ 2
TEST SEL. 200 MHZ
BAND 1 SEL.
BAND 2 SEL.
200 MHZ L.P.F.
PRE-AMP
1 MΩ
ISOLATION AMP
MIXER
X1-X2 FREQ. MULT.
BUFFER
B2 LOCK DETECTOR
CONTROL CIRCUIT
B1 LOCK DETECTOR
LOCK
INT
P.I.A.
BAND 1
10 HZ - 100 MHZ
1M - 20 PF
BAND 2
10 MHZ - 1 GHZ
50Ω NOM
200 MHZ I.F. MAX.
A106 COUNT CHAIN BOARD
BAND 3 SEL.
125 MHZ ± 10 MHZ
SEL B
SEL A
COUNT CHAIN GATE (L)
PULSE FORMING NETWORK
MULTI BAND SELECTOR
1 HZ
10 HZ
100 HZ
ECL HI-FREQ ÷ 10
÷ 10 COUNTER
÷ 10 COUNTER
1 KHZ - 999,999 MHZ
9 DECADE COUNTER 8 DECADE LATCH/MUX
COUNTER OVERFLOW
BUFFER
REAR PANEL
I.F. OUTPUT
RESET
REAL TIME CLOCK
100 mS
100 KHZ
A107 GATE GEN.
ECL GATE CONTROL
BUFFER
100 KHZ
PROG. ATTN. COMP. & LATCH
15db
÷ 100
BUFFER AMP
÷ 2
PROGRAMMABLE TIME BASE 10 μS - 100 SEC.
CONTROL LOGIC
10 MHZ TCXO OSC.
REAR PANEL
10 MHZ IN/OUT
INT
EXT
GATE COMPLETE
I.F. THRESHOLD (L)
A108 CONV. CONT.
VCO REFERENCE
VCO ON/OFF CONT
VCO LOOP FILTER
LOOP FILTER
LOCK DETECT
50 KHZ
YIG CURRENT DRIVER AMP
Ø DETECT
PROG. DIVIDER
14 BIT DAC YIG DRIVER
A105 μ PROCESSOR BOARD
MCM 6802 PROCESSOR
4 MHZ XTAL
SYSTEM CONTROL LOGIC
BUFFER
SYSTEM PROM 16K X 8
SYSTEM RAM 1K X 8
DATA BUS 8
ADDRESS BUS 16
CONTROL BUS 7
MICROPROCCESSOR BUS
FRONT PANEL BOARD A110/111
INT LOGIC
SAMPLE RATE LOGIC
16 X 8 RAM
SCAN CONTROL LOGIC
BUFFERS
CONTROL LOGIC
SEGMENT DRIVERS
KEYBOARD
INT. CONT
2 4 7 1 9 2 5 6 1 9 3
DISPLAY
ANNUNCIATOR
COLUMN DRIVERS
A102A G.P.I.B. OPTION
BUS DRIVERS
MCM 68488 G.P.I.B. CONT. CHIP
ADDRESS SWITCH
DRIVERS/RECEIVER
CONTROL LOGIC
G.P.I.B. CONN. REAR PANEL
A102B B.C.D. RMT. OPT.
BCD
RMT
CONTROL LOGIC
TRI-STATE BUFFER
DRIVERS/RECEIVER
B.C.D. CONN.
REMOTE CONN.
REAR PANEL
P.I.A.
OPTION BOARD A103
OPTION BOARD A104
POWER SUPPLY A101
+5V
-5.2V
+12V
-12V
+18V UNREG
5510057 - B

Figure 9-1. 545A/548A Block Diagram

A100
COUNTER INTERCONNECT
(202180)

FUNCTIONAL
DESCRIPTION
NOT REQUIRED

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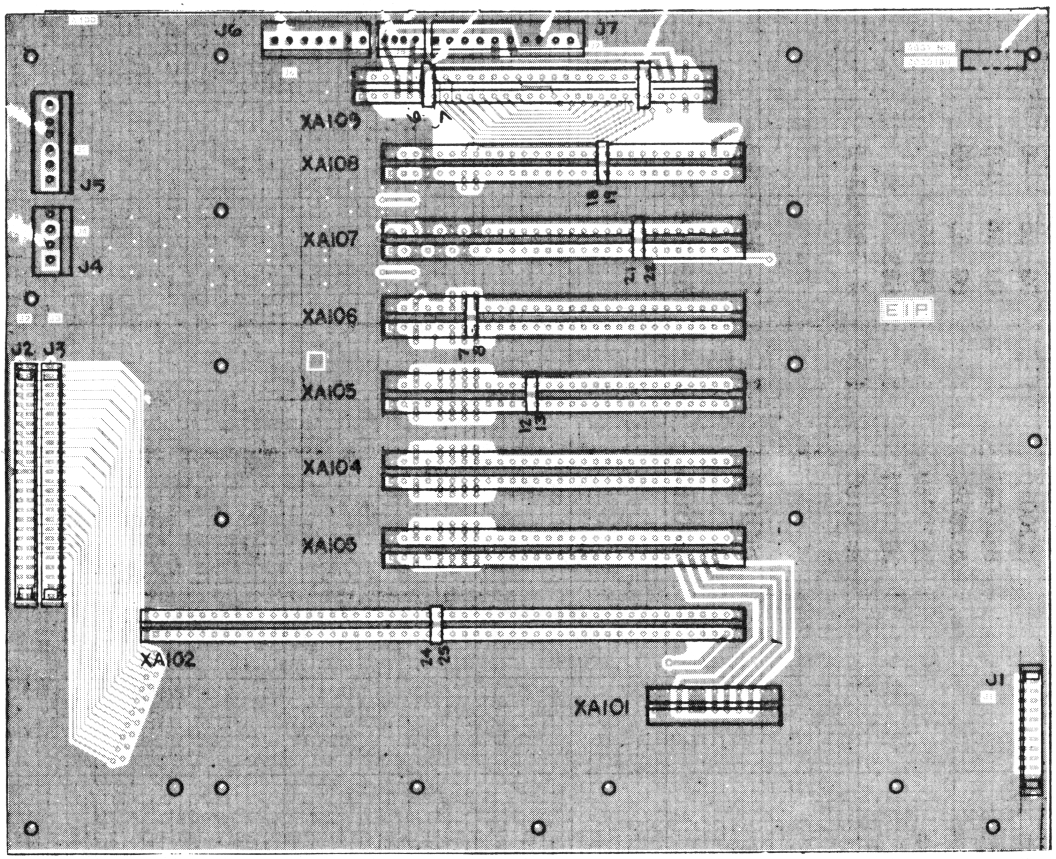
A100 COUNTER INTERCONNECT ASSY

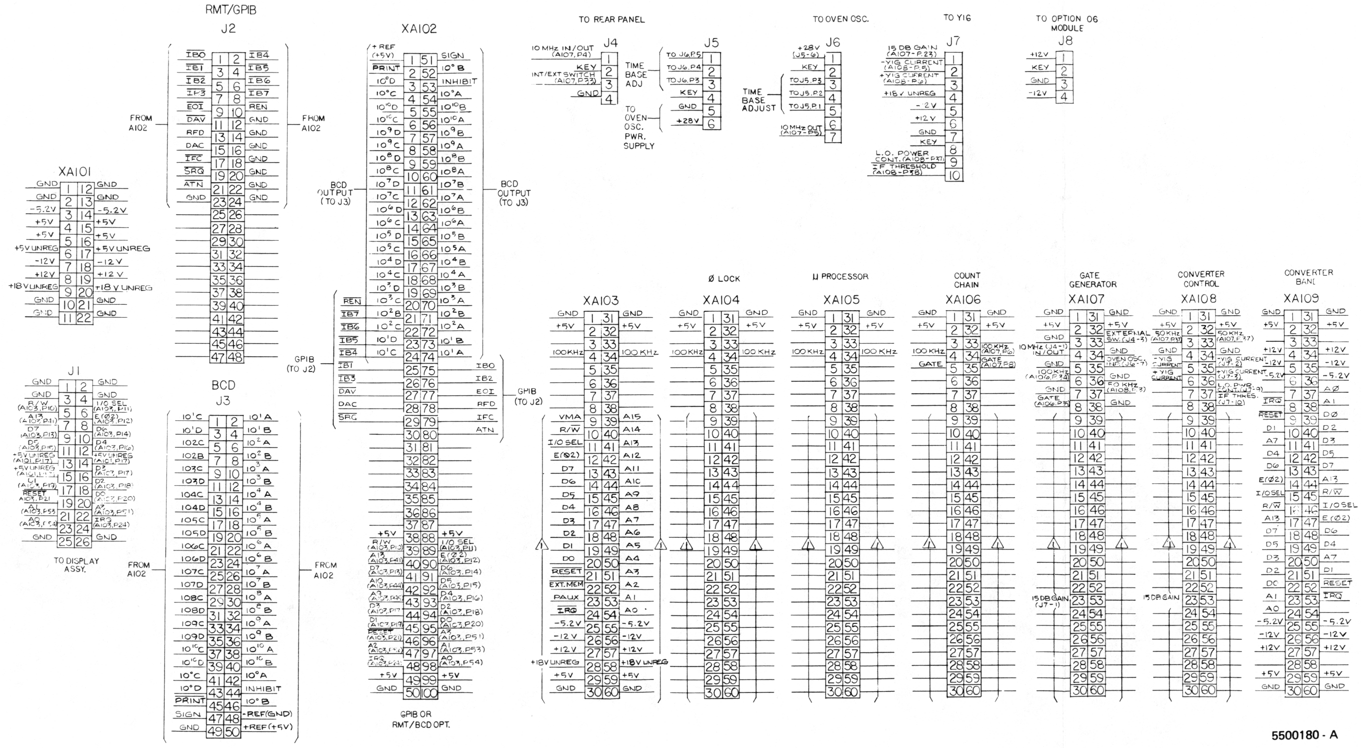
2020180 - B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A100	Counter Interconnect Assy	2020180	1		
J1	Header, Str, 26 pin	2620078	1	3429 - 2302	76381
J2	Header, Str, 50 pin	2620081	2	3433 - 2302	76381
J3	J2				
J4	Friction Lock, 4 pin	2620061	1	09 - 65 - 1049	0000A
J5	Friction Lock, 6 pin	2620090	1	09 - 65 - 1069	"
J6	Header, Str, 7 pin	2620186	1	09-64-1071	"
J7	Header, Str, 10 pin	2620187	1	09-64-1101	"
J8	Friction Lock, 4 pin	2620068	1	640456-4	AMP
XA101	Conn, 11 position	2620183	1	5193-442-1	AMP
XA102	Conn, 50 position	2620103	1	5193-442-3	"
XA103 thru XA109	Conn, 30 position	2620184	7	5193-442-2	"
	Key Plug	5000155	8	530286 - 2	"


J6
J7
XA109
6
7
XA108
18
19
J5
XA107
21
22
J4
XA106
7
8
EIP
J2
J3
XA105
12
13
XA104
XA103
XA102
24
25
XA101
J1

2020180 - B

Figure 100a. Counter Interconnect Component Locator


RMT/GPIB
J2
XA102
TO REAR PANEL
J4
J5
TO OVEN OSC.
J6
TO YIG
J7
TO OPTION 06 MODULE
J8
TIME BASE ADJ
TO OVEN OSC. PWR. SUPPLY
TIME BASE ADJUST
FROM A102
XA101
BCD OUTPUT (TO J3)
GPIB (TO J2)
J1
TO DISPLAY ASSY.
BCD
J3
GPIB OR RMT/BCD OPT.
Ø LOCK
μ PROCESSOR
COUNT CHAIN
GATE GENERATOR
CONVERTER CONTROL
CONVERTER BANK
XA103
XA104
XA105
XA106
XA107
XA108
XA109
5500180 - A

⚠ XA103 THRU XA106 HAVE COMMON CONNECTIONS ON LINES SHOWN IN BRACKETS.

Figure 100b. Counter Interconnect Schematic

A101
POWER SUPPLY
(2020131)

The power Supply furnishes all basic operating voltages required by the counter. The supply consists of two basic sub-assemblies.

- PC Board (A101), containing the rectifiers, filter capacitors, and regulator circuitry.
- Chassis mounted components consisting of the power transformer (T1), primary wiring, F1 fuse; (100/120V), the 220/240V power programming switch; and the on/off power switch (S101) mounted on the front panel.

The basic voltages required by the counter are unregulated +18V, regulated +5V, −5.2, +12V and −12V.

The input AC voltage is full wave rectified and filtered to produce DC voltages of +9V and 18V.

The unregulated +18V is used directly as one supply voltage. The +18V is regulated to a +12V by the action of LM305, a series pass transistor (MJE3055), and foldback current limiting circuitry. The +18V is regulated to a −12V by LM304, a series pass transistor, and foldback current limiting circuitry.

The +9V current is regulated to +5V by a three terminal regulator containing current and thermal sensing circuitry. The +9V current is also regulated to −5.2V by a three terminal regulator that contains thermal and current shutdown circuitry.

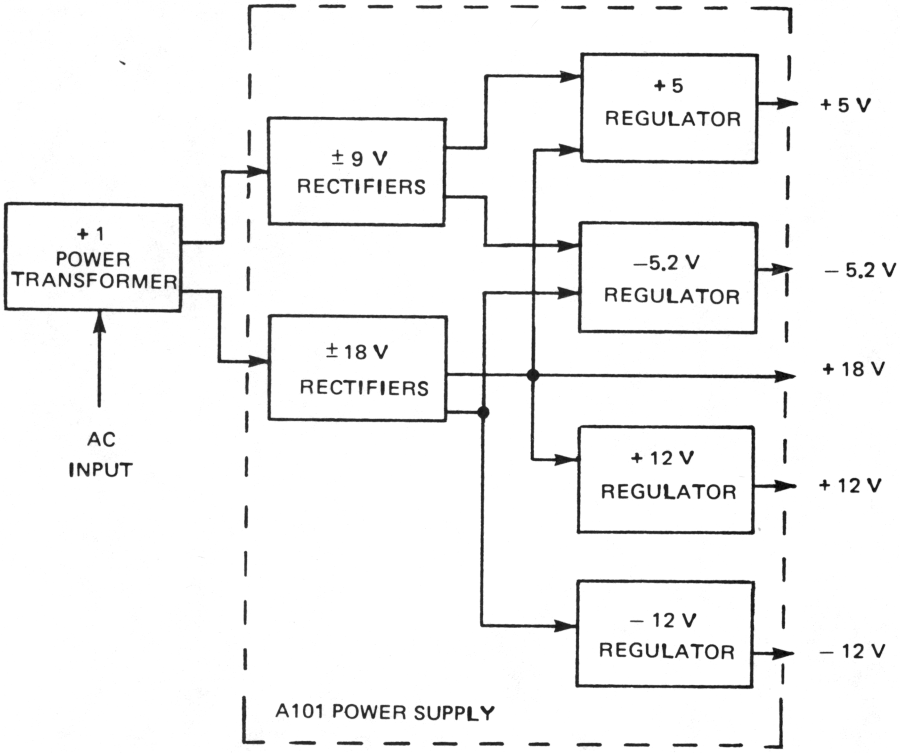
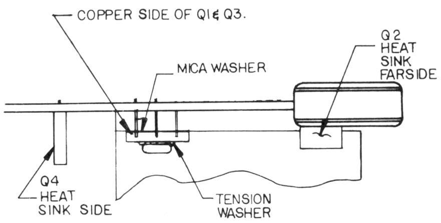

+1
POWER
TRANSFORMER
AC
INPUT
±9 V
RECTIFIERS
±18 V
RECTIFIERS
+5
REGULATOR
−5.2 V
REGULATOR
+12 V
REGULATOR
− 12 V
REGULATOR
+5 V
− 5.2 V
+ 18 V
+ 12 V
− 12 V
A101 POWER SUPPLY

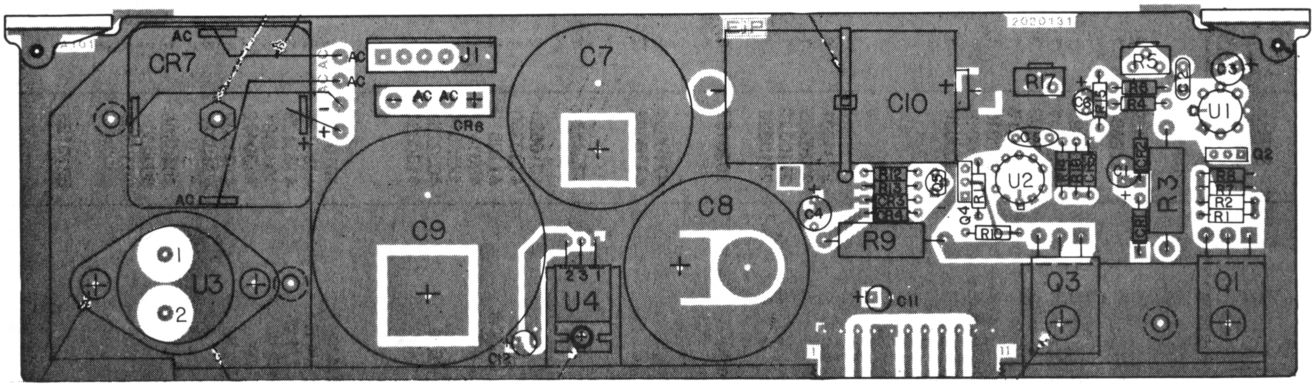
Figure 101a. Power Supply Functional Diagram

A101 POWER SUPPLY ASSY

2020131-B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A101	Power Supply Assy	2020131	1		
C1	Tant. 10μF. 20%, 25V	2300029	2	TAG 20 - 10/25(M)	14433
C2	Mica, 47 pF, 5%, 500V	2260004	1	DM10 - 470J	72136
C3	C1				
C4	Tant, 33μF, 20%, 20V	2300023	1	TAG 20 - 33/20 - 20	14433
C5	Cer, .001μF, 20%, 20V	2150001	1	5GA - D10	56289
C6	Tant, 1.0μF, 20% 35V	2300008	3	TAG 20 -1.0/35 - 50	14433
C7	Elec, 14,000μF, 25V	2200017	1	3110HB143U025	80031
C8	Elec, 9,500μF, 15V	2200016	1	3110HA952U025	80031
C9	Elec, 32,000μF, 15V	2200019	1	3110RB323U015	80031
C10	Elec, 4,700μF, 16V	2200020	1	3050JJ4720U16B	80031
C11	C6				
C12	C6				
CR1 thru CR4	Rectifier	2704001	4	IN4001	07263
CR5	Zener, 12V	2720963	1	IN963A	04713
CR6	Rectifier Brdg	2710029	1	MDA970 - 1	04713
CR7	Rectifier, Brdg	2710028	1	MDA990 - 1	04713
J1	Conn, 6 pin (FRCTN Lock)	2620157	1	640445-6	0000A
Q1	NPN Power	4710001	2	MJE3055	04713
Q2	PNP Power	4710002	2	MJE370	04713
Q3	Q1				
Q4	Q2				
Q5	PNP, General Purpose	4704126	1	2N4126	04713
R1	Comp, 68 ohms, 5%, 1/4 W	4010680	2	RC07GF680J	81349
R2	Met Ox, 36 ohms, 2%, 1/4 W	4130360	1	C4/2%/36	24546
R3	Wire Wound, .66 ohms, 3%, 4W	4110012	2	RS - 2	91637
R4	Prec, 14.7K ohms, 1%, 1/8 W	4061472	1	RN55D1472F	81349
R5	Var. Cer., 500 ohm	4250014	1	72XR500	73138
R6	Prec, 2.26K ohms, 1%, 1/8 W	4062261	1	RN55D2261F	81349
R7	Met Ox, 820 ohms, 2%, 1/4 W	4130821	2	C4/2%/820	24546
R8	R7				
R9	R3				
R10	R1				
R11	Comp, 100 ohms, 5%, 1/4 W	4010101	1	RC07GF101J	81349
R12	Met Ox, 910 ohms, 2%, 1/4 W	4130911	2	C4/2%/910	24546
R13	Met Ox, 12K ohms, 2%, 1/4 W	4130123	1	C4/2%/12K	24546
R14	Prec, 2.43K ohms, 1%, 1/8 W	4062431	1	RN55D2431	81349
R15	Prec, 4.7K ohms, 2%, 1/4 W	4130472	1	C4/2%/4.7	24546
R16	Met Ox, 1K ohms, 2%, 1/4 W	4130102	1	C4/2%/1K	24546
R17	Var, Cer, 2K ohms	4250016	1	72XR2K	73138
U1	Voltage Regulator	3040305	1	LM305	0000X
U2	Voltage Regulator	3040304	1	LM304	0000X
U3	+5VDC Regulator	3057805	1	UA78H05A	07263
U4	-5.2 V Regulator	3057905	1	MC7905.2 CT	04713
	Heatsink	5210196	1	EIP	


COPPER SIDE OF Q1 & Q3.
MICA WASHER
Q2
HEAT
SINK
FARSIDE
Q4
HEAT
SINK SIDE
TENSION
WASHER


CR7
AC
AC
AC
J1
AC AC
CR6
C7
C9
C10
C8
C4
R9
R12
R13
CR3
CR4
Q5
Q4
R11
R10
U2
C5
R16
R15
CR5
R17
R5
R6
R4
C6
R14
C2
Q3
U1
C1
CR2
R3
CR1
Q2
R8
R7
R2
R1
U3
1
2
U4
2 3 1
C12
C11
Q3
Q1
2020131

2020131 - C

Figure 101 b. Power Supply Component Locator

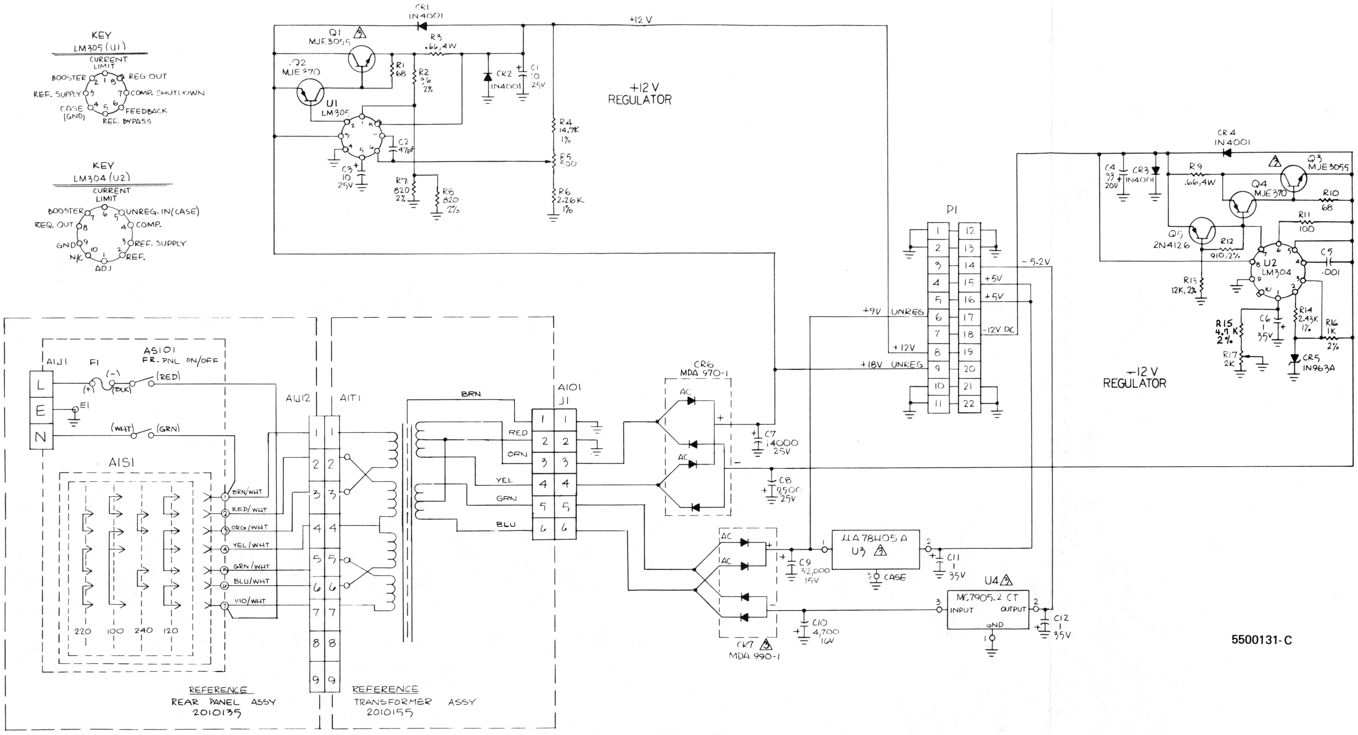

KEY
LM305 (U1)
CURRENT LIMIT
BOOSTER
REG OUT
REF. SUPPLY
COMP. SHUTDOWN
CASE (GND)
FEEDBACK
REF. BYPASS
KEY
LM304 (U2)
CURRENT LIMIT
BOOSTER
UNREG. IN (CASE)
REG. OUT
COMP.
GND
REF. SUPPLY
N/C
REF.
ADJ
CR1 IN4001
+12 V
Q1 MJE3055
Q2 MJE370
R3 .66,4W
R1 68
R2 36 2%
CR2 IN4001
C1 10 25V
U1 LM305
C2 47pF
C3 10 25V
R7 820 2%
R8 820 2%
R4 14.7K 1%
R5 500
R6 2.26K 1%
+12 V REGULATOR
CR4 IN4001
C4 33 20V
CR3 IN4001
R9 .66,4W
Q3 MJE3055
Q4 MJE370
R10 68
R11 100
Q5 2N4126
R12 910,2%
U2 LM304
C5 .001
R13 12K,2%
R15 4.7K 2%
C6 1 35V
R14 2.43K 1%
R16 1K 2%
R17 2K
CR5 IN963A
-12 V REGULATOR
P1
-5.2V
+5V
+5V
-12V DC
+9V UNREG
+12V
+18V UNREG
CR6 MDA 970-1
AC
AC
C7 14000 25V
C8 9500 25V
A1J1
F1
AS101 FR. PNL ON/OFF
(RED)
(BLK)
(WHT)
(GRN)
E1
L
E
N
A1S1
BRN/WHT
RED/WHT
ORG/WHT
YEL/WHT
GRN/WHT
BLU/WHT
VIO/WHT
220
100
240
120
A1J12
A1T1
BRN
RED
ORN
YEL
GRN
BLU
A101 J1
REFERENCE REAR PANEL ASSY 2010135
REFERENCE TRANSFORMER ASSY 2010155
AC
AC
C9 32,000 15V
μA 78H05A U3
CASE
C11 1 35V
U4
MC7905.2 CT
INPUT
OUTPUT
GND
C10 4,700 16V
C12 1 35V
CR7 MDA 990-1
5500131-C

Figure 101c. Power Supply Schematic

△ CR7,Q1,Q3, ,U3 & U4 ARE MOUNTED ON HEATSINKS.

A105
MICROPROCESSOR
(2020195)

In the normal fetch and execute cycle, the microprocessor executes the command sequence stored in the PROMs and, coupled with it's I/O capability, obtains complete control over the counter.

The Microprocessor assembly (A105) is sectioned into four functions as follows:

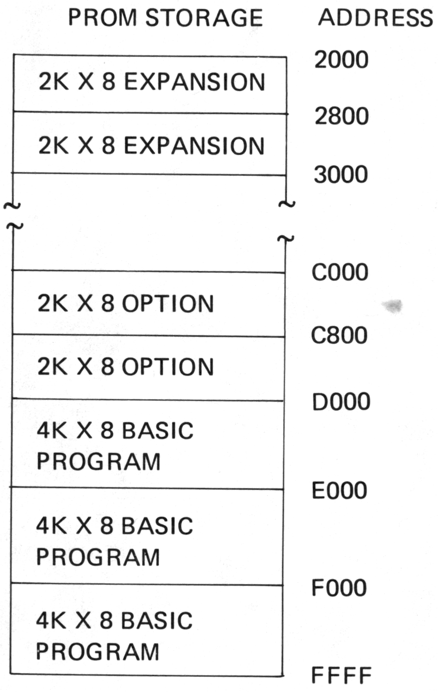
1. Microprocessor
2. Memory elements
3. Power-up reset circuit
4. Control logic and buffers

MICROPROCESSOR

The MCM6802 microprocessor (U1) is used as the main controlling element for the counter. It is driven by a 4 MHz crystal and controls all counter functions by means of a stored program in PROM.

MEMORY ELEMENTS

The memory elements consist of two 1K X 4 RAMs (U6, U7) that are configured to give a total of 1K X 8 storage locations. The basic program for the counter is stored in three 4K X 8 PROMs (U13, U15, U17). Option programs are stored in two 2K X 8 PROMs (U14, U16) and expansion PROMs U19, U20 give the microprocessor board the capability of 20K X 8 total locations for program storage. The memory map for the PROMs is as follows :


PROM STORAGE
ADDRESS
2K X 8 EXPANSION
2K X 8 EXPANSION
2K X 8 OPTION
2K X 8 OPTION
4K X 8 BASIC PROGRAM
4K X 8 BASIC PROGRAM
4K X 8 BASIC PROGRAM
2000
2800
3000
C000
C800
D000
E000
F000
FFFF

POWER-UP RESET CIRCUIT

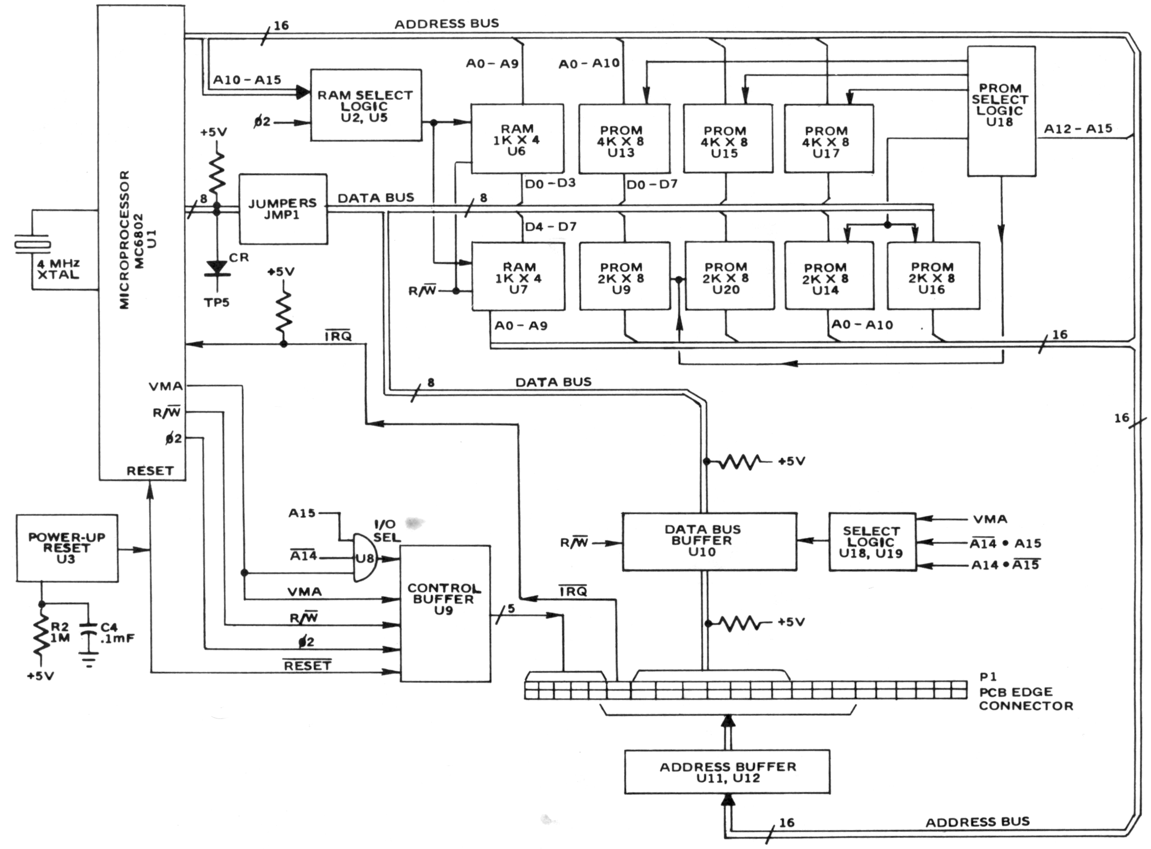
The power-up reset circuit consists of comparator U3 and it's associated components. Resistor R5 provides hysterysis action for the circuit while CR1 provides a path for fast decay time of capacitor C4.

CONTROL LOGIC AND BUFFERS

The I/O select line is used to enable I/O chips associated with the processor system. The equation for the selection of I/O is :

$$I/O\ SEL = VMA \bullet A15 \bullet \overline{A14}$$

The three busses which are brought out of the microprocessor board are the 16 bit address bus, the 8 bit data bus, and the 6 bit control bus. Buffer/Driver chips U9, U10, U11, U12 provide drive current that is sufficient to drive the external bus.



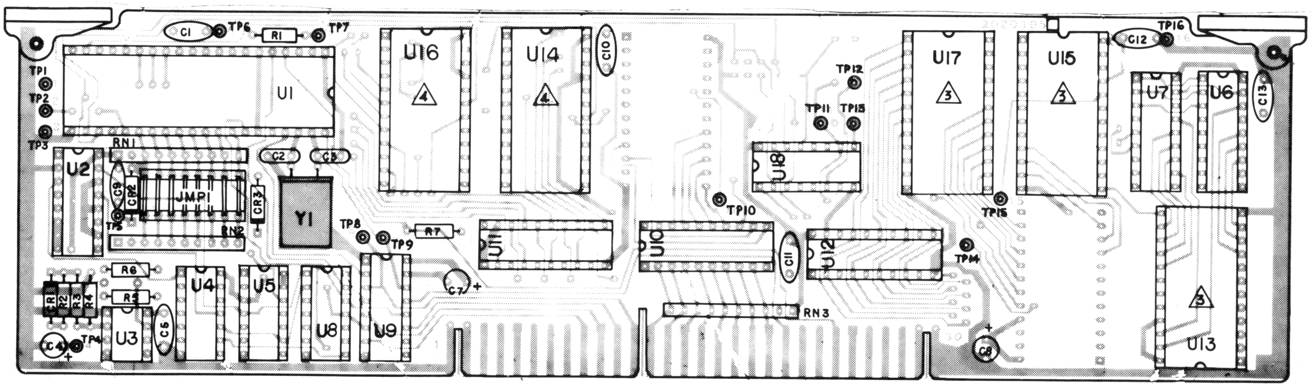
16
ADDRESS BUS
A10 - A15
RAM SELECT LOGIC U2, U5
ϕ2
A0 - A9
A0 - A10
PROM SELECT LOGIC U18
A12 - A15
+5V
RAM 1K X 4 U6
PROM 4K X 8 U13
PROM 4K X 8 U15
PROM 4K X 8 U17
MICROPROCESSOR MC6802 U1
8
JUMPERS JMP1
DATA BUS
8
D0 - D3
D0 - D7
D4 - D7
4 MHz XTAL
CR
TP5
+5V
R/W̄
RAM 1K X 4 U7
PROM 2K X 8 U9
PROM 2K X 8 U20
PROM 2K X 8 U14
PROM 2K X 8 U16
A0 - A9
A0 - A10
16
IRQ
VMA
R/W̄
ϕ2
RESET
8
DATA BUS
16
+5V
POWER-UP RESET U3
A15
I/O SEL
A14
U8
VMA
R/W̄
ϕ2
RESET
CONTROL BUFFER U9
5
IRQ
R/W̄
DATA BUS BUFFER U10
SELECT LOGIC U18, U19
VMA
A14 • A15
A14 • A15
+5V
R2 1M
C4 .1mF
+5V
P1 PCB EDGE CONNECTOR
ADDRESS BUFFER U11, U12
16
ADDRESS BUS

Figure 105a. Microprocessor Assembly A105

A105 MICROPROCESSOR

2020195 - A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A105	Microprocessor Assy	2020195	1	EIP	
C1	Cer, .01μF, 20%, 100V	2150003	7	TG - S10	56289
C2	Mica, 12pF, 5%, 500V	2260013	1	CD10CD120J03	72136
C3	Mica, 15pF, 5%, 500V	2260014	1	CD10CD150J03	72136
C4	Tant, 0.1μF, 20%, 35V	2300020	1	TAPA 0.1M35	14433
C5	C1				
C6	Not used				
C7	Tant, 33μF, 20%, 10V	2300015	2	TAPA 33M10	14433
C8	C7				
C9 thru C13	C1				
CR1 thru CR3	Hot Carrier	2710004	3	FH 1100	07263
R1	Comp, 10K, 5%, 1/8W	4010103	2	RC07GF103J	81349
R2	Comp, 1M, 5%, 1/8W	4010105	1	RC07GF105J	81349
R3	R1				
R4	Comp, 4.3K, 5%, 1/8W	4010432	1	RC07GF432J	81349
R5	Comp, 22K, 5%, 1/8W	4010223	1	RC07GF223J	81349
R6	Comp, 4.7K, 5%, 1/4W	4010472	2	RC07GF472J	81349
RN1 thru RN3	Network, 10K	4170003	3	785-1-R10K	80740
TP1 thru TP16	Conn, Pin, .04D, Gold	2620032	16	460-2970-02-03	71279
U1	MPU W/CLK-RAM	3056802	1	MC6802	04713
U2	6 Bit Comparator	3078136	1	DM8136	27014
U3	Voltage Comparator	3050311	1	LM311N	0000X
U4	Hex Inverter	3087404	1	DM74LS04	0000X
U5	3-INP NAND Gate	3087410	1	DM74LS10	0000X
U6	1K x 4 Bit RAM	3052114	2	2114	EM&M
U7	U6				
U8	3-INP AND Gate	3087411	1	DM74LS11N	0000X
U9	Hex Buss Driver/Buffer	3084365	1	SN74LS365N	01295
U10	Octal Buss Transceiver	3084245	1	SN74LS245N	01295
U11	Line Driver/Octal Buffer	3084244	2	SN74LS244N	01295
U12	U11				
U13	PROM, Basic Counter	2060002-01	Ref	6500001-XX	
U14	PROM, Band 4 Option	2060002-06	Ref	6400002-01	
U15	U13				
U16	PROM, GPIB Option	2060002-02	Ref	6400002-02	
Alt. U16	PROM, BCD/RMT Option	2060002-05	Ref	6400002-03	
U17	U13				
U18	2-4 Lie Decoder/DE Mult.	3084139	1	SN74LS139N	01295
Y1	4 MHz Crystal	2030015	1	MP1PR400	

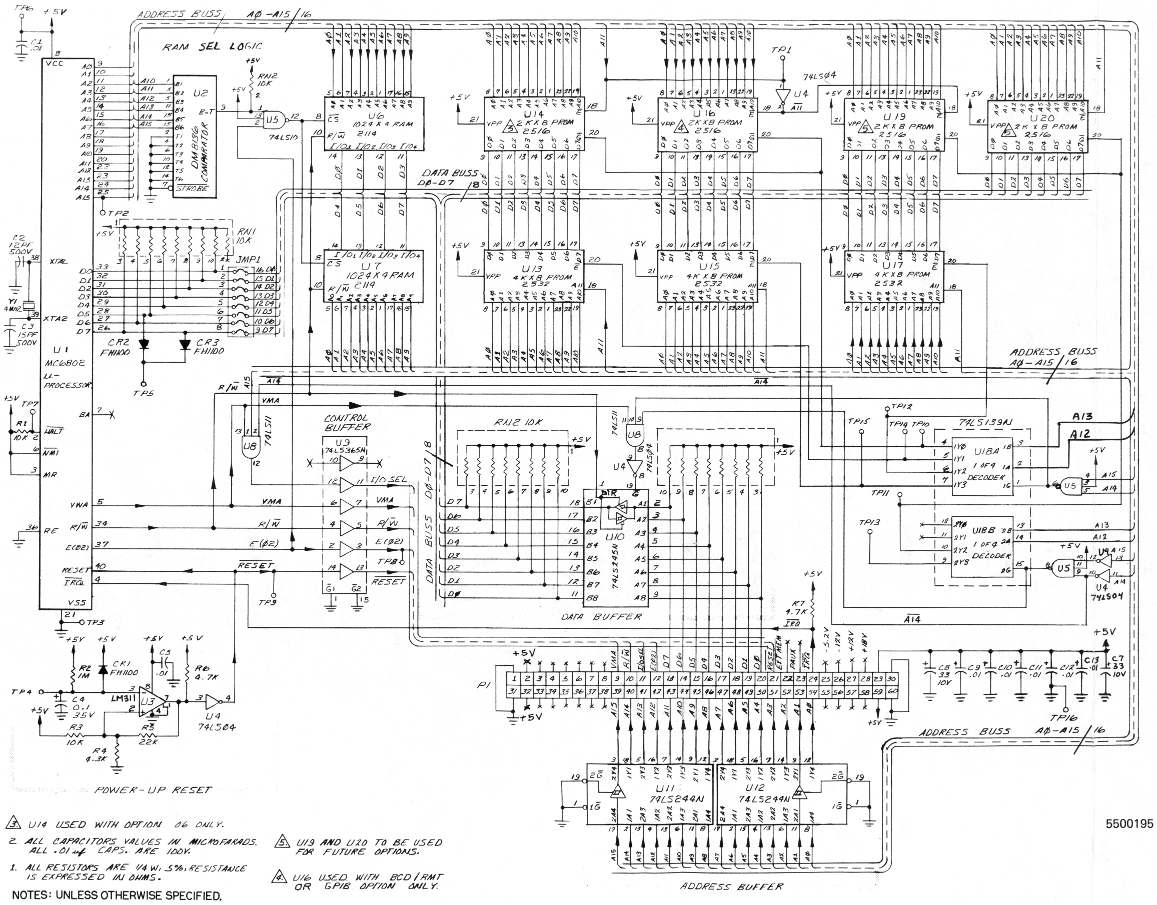

C1
TP6
R1
TP7
U16
4
U14
4
C10
U17
3
U15
3
C12
TP16
TP1
TP2
TP3
U1
TP12
TP11
TP13
U7
U6
C13
RN1
C2
C3
U2
C9
CR2
JMP1
CR3
Y1
TP5
RN2
U18
TP10
TP15
TP8
TP9
R7
U11
U10
C11
U12
TP14
R6
R5
CR1
R2
R3
R4
U4
U5
U8
U9
C7
RN3
U3
C5
C4
TP4
C8
3
U13

△4 U14 & U16 INSTALLED AT OPTION ASSEMBLIES.

△3 PROM SET (U13, U15 & U17) INSTALLED AT BASIC COUNTER ASSY.

5500195 - A

Figure 105c. Microprocessor Component Locator


ADDRESS BUSS A0-A15 16
RAM SEL LOGIC
U1 MC6802 µP-PROCESSOR
U2 DM8136 COMPARATOR
U5 74LS10
U6 1024 X 4 RAM 2114
U7 1024 X 4 RAM 2114
U14 2K X 8 PROM 2516
U16 2K X 8 PROM 2516
U19 2K X 8 PROM 2516
U20 2K X 8 PROM 2516
U13 4K X 8 PROM 2532
U15 4K X 8 PROM 2532
U17 4K X 8 PROM 2532
DATA BUSS D0-D7 8
RN1 10K
JMP1
CR2 FH1100
CR3 FH1100
Y1 4 MHZ
CONTROL BUFFER
U9 74LS365N
I/O SEL
VMA
R/W
E(Ø2)
RESET
IRQ
RN2 10K
U8 74LS11
U10 74LS245N
DATA BUFFER
74LS139N
U18A 1 OF 4 DECODER
U18B 1 OF 4 DECODER
U4 74LS04
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TP10
TP11
TP12
TP13
TP14
TP15
TP16
P1
U11 74LS244N
U12 74LS244N
ADDRESS BUFFER
LM311
U3
CR1 FH1100
POWER-UP RESET

△3. U14 USED WITH OPTION 06 ONLY.

2. ALL CAPACITORS VALUES IN MICROFARADS. ALL .01 µf CAPS. ARE 100V.

1. ALL RESISTORS ARE 1/4 W, 5%, RESISTANCE IS EXPRESSED IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED.

△5. U19 AND U20 TO BE USED FOR FUTURE OPTIONS.

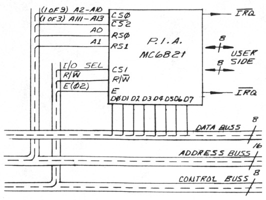
△4. U16 USED WITH BCD/RMT OR GPIB OPTION ONLY.

MEMORY ADDRESS CHART	
ADDRESS	IC
0000 03FF	U6, U7
D0000 DFFF	U13
C000 C7FF	U14
F000 FFFF	U15
C800 CFFF	U16
E000 EFFF	U17
2800 2FFF	U19
2000 27FF	U20

HIGHEST REF. DES.							
TP16	C13	CR3	R7	RN3	JMP1	U18	Y1
REF. DES. NOT USED							

IC NO.	TYPE	PIN NO. GND	PIN NO. +5V
U1	MC6802	1, 21	8, 35
U2	DM8136	8	16
U8	74LS11	7	14
U4	74LS04	7	14
U6, U7	1024 X 4 RAM 2114	9	18
U13, 15, 17	4K X 8 PROM 2532	12	24
U14, 16, 19, 20	2K X8 PROM 2516	12	24
U18	74LS139	8	16
U10	74LS245	10	20
U3	LM311N	1, 4	8
U11, U12	74LS244	10	20
U5	74LS10	7	14
U9	74LS365	8	16

TYPICAL P.I.A. I/O CONNECT
(REF. ONLY.)


(1 OF 9) A2-A10
(1 OF 3) A11-A13
A0
A1
I/O SEL
R/W
E(Ø2)
CS0
CS2
RS0
RS1
CS1
R/W
E
D0 D1 D2 D3 D4 D5 D6 D7
P.I.A. MC6821
IRQ
8
8
USER SIDE
IRQ
DATA BUSS 8
ADDRESS BUSS 16
CONTROL BUSS 8

5500195 - A

Figure 105d. Microprocessor Schematic

A106
COUNT CHAIN
(2020136)

The Count Chain Assembly receives IF signals from the Band 3 IF Amplifier (A201B) and the Band 2 Converter (A109). It also receives a gate signal and a 100 kHz reference signal from the Gate Generator (A107). The count chain assembly selects the appropriate IF signal, gates it, and counts it to produce a BCD output that represents the input frequency. It also produces one or two IF output signals to be used for options at J3 and J4.

The A106 board receives two IF input signals on J1 and J2. The appropriate input is selected by enabling one of two differential amplifiers (U1A or U1B). Enabling of the appropriate amplifier is achieved by turning on a transistor switch (Q11 or Q12). The appropriate transistor is turned on by the output of an open collector inverter (U7C or U7A) driven by a TTL signal from the PIA (U10).

The output of the input selector differentially drives a squaring circuit. The squaring circuit consists of a differentially driven current mirror (Q1) driving a tunnel diode (CR5). The voltage across the tunnel diode changes abruptly between two states (approximately 0.2V and 0.5V). The signal across the diode drives the pulse forming circuit. This circuit begins with a high speed differential amplifier (Q2 and Q3). The output of this amplifier drives Q4 which is a current switch. The square wave current, from Q4's collector, drives an inductor (L1). The voltage across the inductor is a series of pulses; a positive pulse when Q4 turns on and a negative pulse when Q4 turns off. Diode CR5 tends to remove the negative pulses and increases the damping to improve the amplitude of the positive pulses. The positive pulses from the generator drive a pulse inverter (Q6). The pulse inverter is a high-speed zero bias amplifier that is biased at cut off by diode CR6.

The output of the pulse inverter (Q6) drives the input to the first decade counter (U2). The bias for the U2 input is established by a tracking bias supply (U3, Q7). The voltage at TP2 is equal to the voltage on U2 pin 1, plus a fixed DC offset selected by R45. The BCD outputs from U2 are slew-rate limited, and can only be seen after the counting ends and comes to rest. The carry output on pin 9 is an ECL level U2 signal, and is always visible.

The ECL output of U2 drives an ECL to TTL converter (Q8, Q9 and Q10). This converter is a differential amplifier with a cascode output buffer (Q8). The response of Q8 is improved by inductive peaking provided by L2. The output of Q8 drives a decade counter (U4) which in turn drives a third decade counter (U5). The BCD outputs of U4 and U5 are connected to a 6 decade counter (U6) which derives its clock information directly from the BCD outputs of U5. When counting is finished, 8 decades of BCD data are read by the microprocessor (through the PIA U10) from U6 by a time multiplex process. The multiplexer (set to the first digit by the end of the previous reset clock) loads the multiplex latches with the $\overline{\text{Latch Load}}$ clock, and steps to the remaining 7 digits with 7 pulses on the $\overline{\text{Scan Clock}}$ line. The first decade of BCD data from U2 is read directly from the PIA.

A single reset line is used to reset all count stages to zero before the next count cycle begins.

A real-time clock (U8, U9) is also on the count chain assembly. This circuit takes the 100kHz reference signal, that is coming from the Counter Interconnect Assembly (A100), and divides it by 10,000 to give a 10Hz (100ms) clock. The output from this clock is fed to the PIA to allow the microprocessor to gather time information at a 10Hz rate for timing functions within the program.

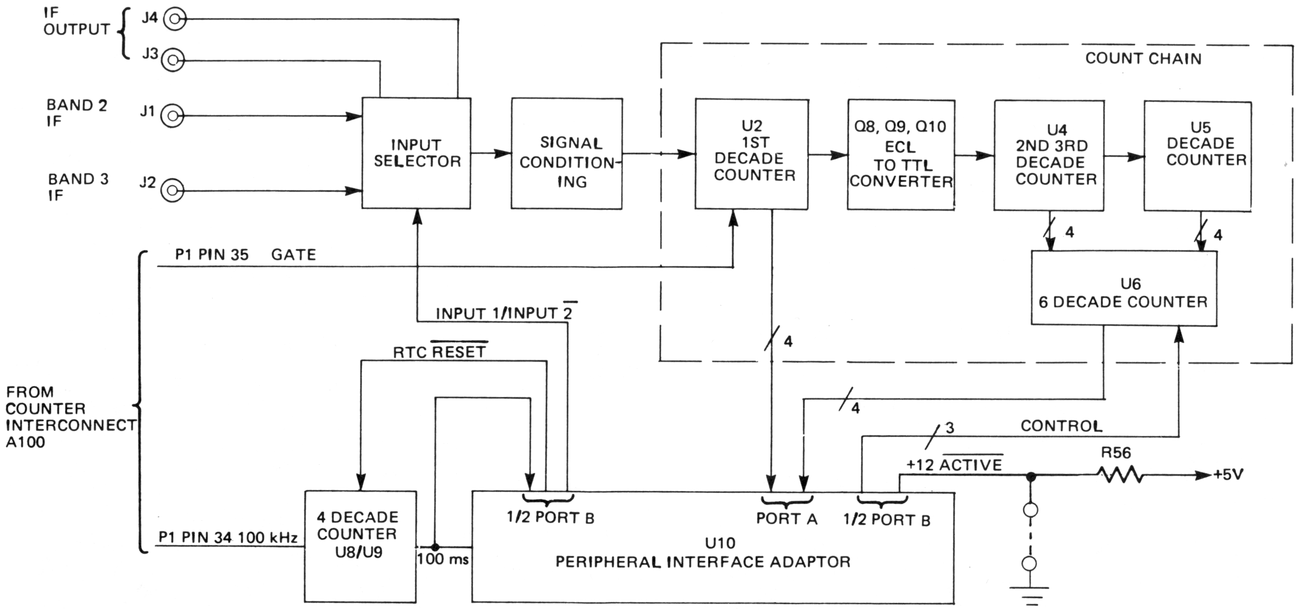

IF OUTPUT
J4
J3
BAND 2 IF
J1
BAND 3 IF
J2
INPUT SELECTOR
SIGNAL CONDITIONING
COUNT CHAIN
U2 1ST DECADE COUNTER
Q8, Q9, Q10 ECL TO TTL CONVERTER
U4 2ND 3RD DECADE COUNTER
U5 DECADE COUNTER
4
4
U6 6 DECADE COUNTER
P1 PIN 35 GATE
INPUT 1/INPUT $\overline{2}$
RTC $\overline{\text{RESET}}$
4
4
3
CONTROL
FROM COUNTER INTERCONNECT A100
+12 $\overline{\text{ACTIVE}}$
R56
+5V
P1 PIN 34 100 kHz
4 DECADE COUNTER U8/U9
100 ms
1/2 PORT B
PORT A
1/2 PORT B
U10 PERIPHERAL INTERFACE ADAPTOR

Figure 106a. Count Chain Functional Diagram

5580021

A106 COUNT CHAIN ASSY

2020136 - G

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A106	Count Chain Assy	2020136	1		
C1	Tant, 33µF, 20%, 10V	2300015	5	TAG 20 - 33/10 - 50	14433
C2	Cer., .01µF, 20%, 100V	2150003	18	TG - S10	56289
C3	C2				
C4	C1				
C5	Mica, 10pF, 5%, 500V	2260012	1	DM15CD100J03	72136
C6	Tant, 10µF, 20%, 25V	2300029	4	DF106M255	NEC
C7	C2				
C8	C2				
C9	Cer., .001µF, 20%, 1KV	2150001	3	5GA - D10	56289
C10	C2				
C11	C2				
C12	C9				
C13	C2				
C14	C6				
C15	C6				
C16	C2				
C17	C9				
C18	Not Used				
C19	Not Used				
C20	C1				
C21	C2				
C22	C1				
C23	Not Used				
C24 thru C28	C2				
C29	C1				
C30 thru C33	C2				
C34	C6				
CR1	General Purpose	2704154	3	IN4154	07263
CR2	Zener, 6.2V	2705234	1	IN5234	04713
CR3	CR1				
CR4	Tunnel, Switching	2710033	1	G00010C	20754
CR5	Hot Carrier	2710016	1	5082 - 2835	28480
CR6	CR1				
CR7	Not Used				
L1	Part of Board				
L2	Inductor, 1µH	3510003	1	DD 1.0	72259
Q1	PNP, RF	4704959	1	2N4959	04713
Q2	NPN, RF SW	4710035	3	SMT 1128	04713
Q3	Q2				
Q4	PNP, RF	4710010	1	MPS - H81	04713
Q5	NPN, RF	4710024	1	BFR90	73445
Q6	NPN, RF	4710026	1	NE73432B	0000S
Q7	Q2				
Q8	NPN, RF	4705179	3	2N5179	04713
Q9	Q8				
Q10	Q8				
Q11	PNP, General Purpose	4704126	2	2N4126	04713
Q12	Q11				

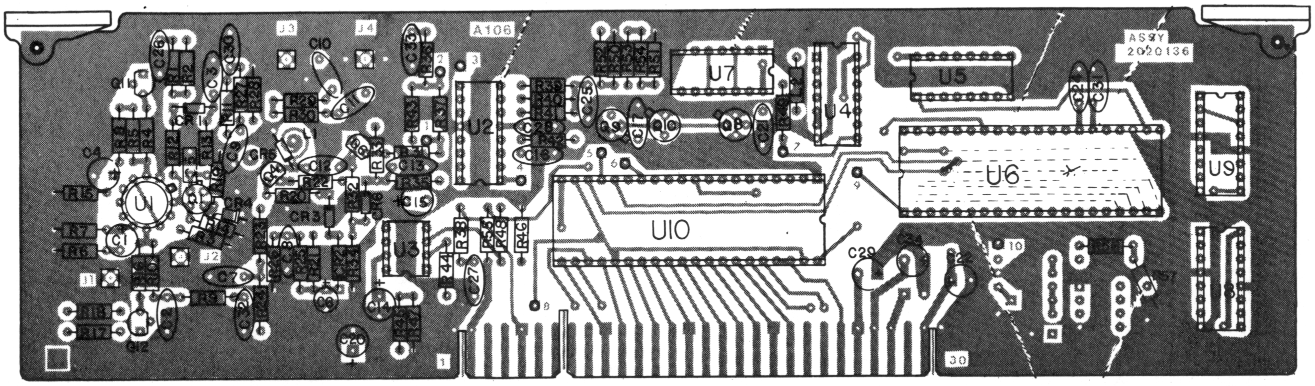
A106 COUNT CHAIN ASSY, continued

2020136- G

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R1	Comp., 1.5K, 5%, 1/4 W	4010152	2	RC07GF152J	81349
R2	Comp., 6.2K, 5%, 1/4 W	4010622	2	RC07GF622J	81349
R3	Comp., 51 ohm, 2%, 1/4 W	4130510	3	C4/2%/51	24546
R4	Comp., 5.1K, 5%, 1/4 W	4010512	2	RC07GF512J	81349
R5	Comp., 2.7K, 5%, 1/4 W	4010272	2	RC07GF272J	81349
R6	Comp., 51 ohm, 5%, 1/4 W	4010510	1	RC07GF510J	81349
R7	Met Ox, 2K, 2%, 1/4 W	4130202	3	C4/2%/2K	24546
R8	Comp., 510 ohm, 5%, 1/4 W	4010511	1	RC07GF511J	81349
R9	Comp., 5.6 ohm, 5%, 1/4 W	4010569	5	RC07GF5R6J	81349
R10	R5				
R11	R9				
R12	Met Ox, 68 ohm, 2%, 1/4 W	4130680	1	C4/2%/68	24546
R13	Met Ox, 43 ohm, 2%, 1/4 W	4130430	1	C4/2%/43	24546
R14	Met Ox, 3.9K, 2%, 1/4 W	4130392	1	C4/2%/3.9K	24546
R15	R7				
R16	R4				
R17	R1				
R18	R2				
R19	Comp., 100 ohm, 5%, 1/4 W	4010101	1	RC07GF101J	81349
R20	Met Ox, 56 ohm, 2%, 1/4 W	4130560	2	C4/2%/56	24546
R21	R9				
R22	R20				
R23	Comp., 430 ohm, 5%, 1/4 W	4010431	1	RC07GF431J	81349
R24	R9				
R25	Met Ox, S.A.T. (2K, 2% Nom)	4130999	1	C4/2%/XX	24546
R26	Met Ox, 39 ohm, 2%, 1/4 W	4130390	2	C4/2%/39	24546
R27	Met Ox, 200 ohm, 2%, 1/4 W	4130201	3	C4/2%/200	24546
R28	Met Ox, 270 ohm, 2%, 1/4 W	4130271	1	C4/2%/270	24546
R29	R3				
R30	R3				
R31	Comp, 10 ohm, 5%, 1/4 W	4010100	2	RC07GF100J	81349
R32	Met Ox, 47 ohm, 2%, 1/4 W	4130470	1	C4/2%/47	24546
R33	Met Ox, 20 ohm, 2%, 1/4 W	4130200	1	C4/2%/20	24546
R34	Met Ox, 510 ohm, 2%, 1/3 W	4130511	1	C4/2%/510	24546
R35	R9				
R36	Met Ox, 1K, 2%, 1/4 W	4130102	3	C4/2%/1K	24546
R37	R26				
R38	Comp., 390 ohm, 5%, 1/4 W	4010391	1	RC07GF391J	81349
R39 thru R42	Comp, 10 K, 5%, 1/4 W	4010103	4	RC07GF103J	81349
R43	Met Ox, 20 K, 2%, 1/4 W	4130203	4	C4/2%/20K	24546
R44	R43				
R45	R36				
R46	R43				
R47	Met Ox, 18 ohm, 2%, 1/4 W (NOM) SAT	4130999	1	C4/2%/18	24546
R48	R43				
R49	Met Ox, 240 ohm, 2%, 1/4 W	4130241	1	C4/2%/240	24546
R50	R27				
R51	R27				
R52	R36				
R53	Met Ox, 430 ohm, 2%, 1/4W	4130431	1	C4/2%/430	24546

A106 COUNT CHAIN ASSY, continued

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R54	R7				
R55	Comp., 1.8K, 5%, 1/4 W	4010182	1	RC07GF182J	81349
R56	Comp., 4.7K 5%, 1/4 W	4010472	1	RC07GF472J	81349
R57	R31				
TP1 thru TP10	Conn., Pin, .040D	2620032	10	460-2970-0203	71279
U1	Dual/Diff Ampl	3043049	1	CA3049T	07263
U2	UHF, BCD, Decade Counter	3010637	1	SP8637B	0000C
U3	Op Amplifier	3040741	1	LM741CN	0000X
U4	PST Decade Counter	3084196	1	SN74LS196N	01295
U5	4 Bit Decade Counter	3084160	1	SN74LS160N	01295
U6	6 Dec. Ctr/8 Dec. Latch	3057031	1	LS74031	01295
U7	Hex Inverter	3087404	1	DM74LS04N	0000X
U8	Decade Counter	3084490	2	74LS490N	01295
U9	U8				
U10	Periph. Interface Adapter	3086820	1	MC6820	04713


A106
J3
J4
C10
C4
C1
U1
U2
U3
U4
U5
U6
U7
U8
U9
UIO
J2
R15
R7
R6
R16
R17
R9
R20
R22
R29
R30
R33
R35
R38
R40
R44
R46
CR1
CR3
CR4
CR5
C7
C12
C13
C15
C16
C28
C29
C24
C22
C27
C25
C30
C33
Q11
Q12
ASSY
2020136
1
30

2020136 - G

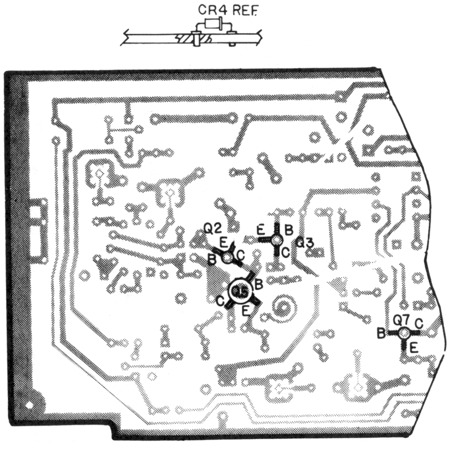
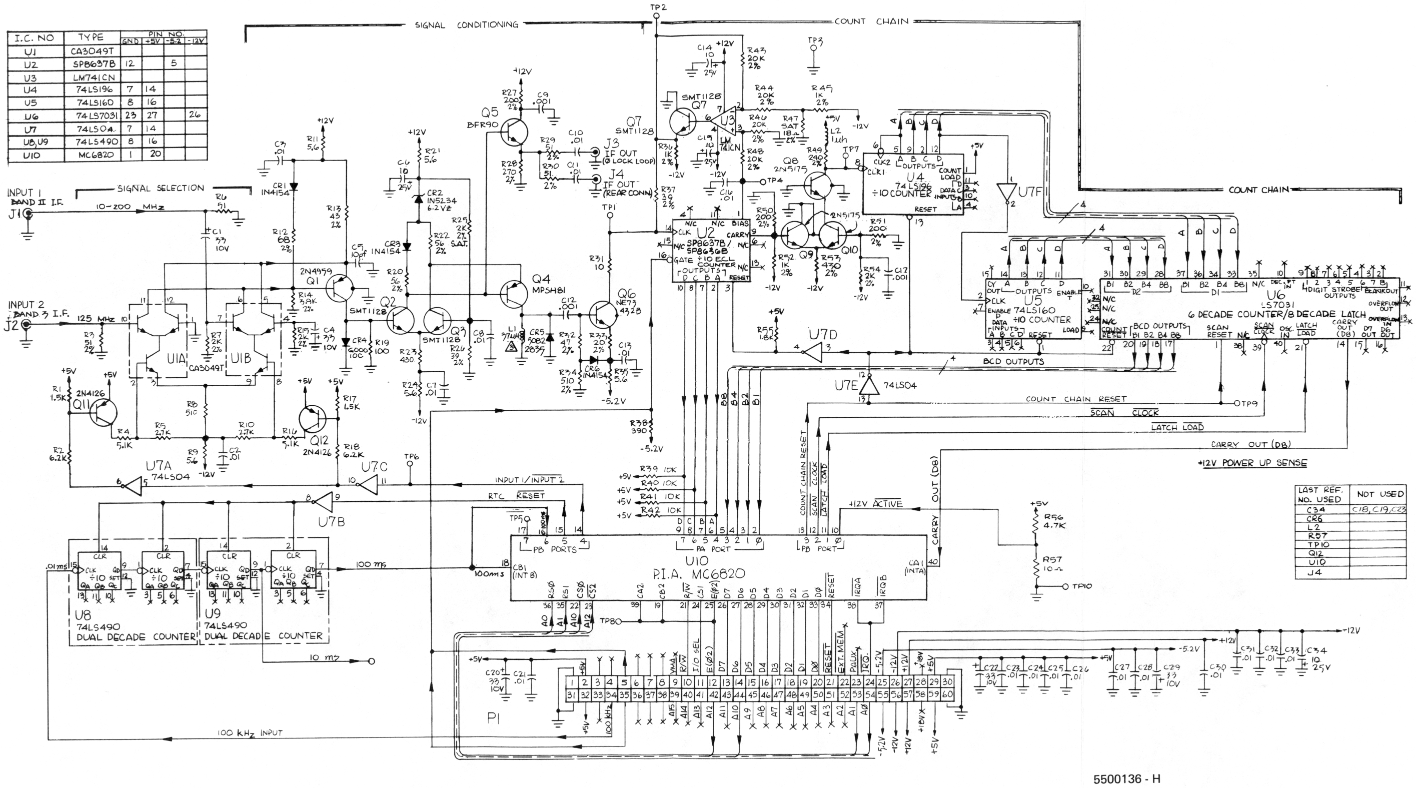

CR4 REF
Q2
E
C
B
E
B
C
Q3
Q5
B
C
E
B
Q7
C
E

Figure 106 b. Count Chain Component Locator


SIGNAL CONDITIONING
TP2
COUNT CHAIN
SIGNAL SELECTION
INPUT 1
BAND II I.F.
J1
10-200 MHz
INPUT 2
BAND 3 I.F.
J2
125 MHz
U1A
U1B
CA3049T
Q1
2N4959
Q2
SMT1128
Q3
SMT1128
Q4
MPSH81
Q5
BFR90
Q6
NE73432B
Q7
SMT1128
Q8
2N5179
Q9
Q10
2N5179
Q11
2N4126
Q12
2N4126
U2
SP8637B/SP8636B
÷10 ECL COUNTER
U3
LM741CN
U4
74LS196
÷10 COUNTER
U5
74LS160
÷10 COUNTER
U6
LS7031
6 DECADE COUNTER/8 DECADE LATCH
U7A
U7B
U7C
U7D
U7E
U7F
74LS04
U8
74LS490
DUAL DECADE COUNTER
U9
74LS490
DUAL DECADE COUNTER
U10
P.I.A. MC6820
J3
IF OUT
(Ø LOCK LOOP)
J4
IF OUT
(REAR CONN)
BCD OUTPUTS
COUNT CHAIN RESET
SCAN CLOCK
LATCH LOAD
CARRY OUT (DB)
+12V POWER UP SENSE
+12V ACTIVE
INPUT 1/INPUT 2
RTC RESET
100 ms
10 ms
100 kHz INPUT
P1
TP9
TP10
-5.2V
+12V
-12V
+5V

I.C. NO	TYPE	PIN NO.			
		GND	+5V	-5.2	-12V
U1	CA3049T				
U2	SP8637B	12		5	
U3	LM741CN				
U4	74LS196	7	14		
U5	74LS160	8	16		
U6	74LS7031	23	27		26
U7	74LS04	7	14		
U8,U9	74LS490	8	16		
U10	MC6820	1	20		

LAST REF. NO. USED	NOT USED
C34	C18, C19, C23
CR6	
L2	
R57	
TP10	
Q12	
U10	
J4	

5500136 - H

⚠ INDUCTOR PART OF P.C. BOARD.

Figure 106c. Count Chain Schematic

A107
GATE GENERATOR
(2020197)

This assembly performs the following functions.

- Reference Oscillator Control
- Gate Generation
- Band 3 Amplitude Determination
- Power Meter Control (Option 02 only)

REFERENCE OSCILLATOR CONTROL

This circuit selects, as the time base for the counter, either the internal reference oscillator or an external 10 MHz signal applied to the rear panel. This circuit provides a 100 kHz TTL level clock signal for the gate generator, a 50 kHz TTL level clock signal for the microwave converter and, in the internal oscillator mode, a 10 MHz signal (1 volt p-p into 50 ohms) to the rear panel.

The 10 MHz internal reference signal is applied to a switchable "analog to TTL" converter (Q1, Q2, Q3). When the Ref Int/Ext line is high the TTL converter is enabled. One output goes to drive Q4, giving a square wave (1V p-p into 50 ohms) on the 10 MHz Ref line. A second output goes to NAND gate U1 (also switchable for signal isolation). The output of U1 goes to the clock input of U2. U2 is a dual decade divider that divides by 100. The output of U2 is a 100 kHz TTL clock signal to the gate generator. The output of U2 also goes through inverter U7 to one half of U17 and provides a 50 kHz TTL signal for the microwave converter.

When the Reference Int/Ext line is set to external (low) the TTL converter (Q1, Q2, Q3) and driver (Q4) are disabled, TTL converter (Q5, Q6, Q7) is enabled, and U1 is set to select the external input. An external reference signal applied to the 10 MHz reference line is then converted to the input of U2.

GATE GENERATOR

The Gate Generator must provide an accurate, stable, signal gate to the Count Chain. The gate must be switchable, in decade increments, between 100 micro sec and 1 sec. The gate generator consists of a programmable divide-by-N time base (U5), a dual flip-flop (U6A, U6B), and an ECL flip flop (U8). The divide ratio of U5, which determines the gate time, is set by U5 pins 12, 13, and 14 as follows.

Pin 12	Pin 13	Pin 14	Divide Ratio	Gate Time
0	0	1	10^1	100 μsec
0	1	0	10^2	1 Msec
0	1	1	10^3	10 Msec
1	0	0	10^4	100 Msec
1	0	1	10^5	1 sec

The outputs of U5 and U6 enable ECL flip-flop U8, but U8 is clocked directly from the 100kHz clock to insure gate accuracy.

When the gate is not active, U5 is permitted to free-run by holding U6A clear (T0). The gate is initialized by setting U6A. This clears U6B and clears U5 (T1). The next clock pulse sets U8 (T2). The gate is then enabled by momentarily clearing U6A (T3). The next clock sets U6B which enables U5 and U8 (T4). At T5 the gate is opened and U5 begins counting clocks (T5). Halfway through the gate, U5 pin 1 goes high (T6). After U5 has accumulated the proper number of clocks its output, pin 1, goes low. This sets U6A, which clears U6B, and sets U8 pin 7 high (T7). The next clock closes the gate (T8). The program next clears U6A (T9), which enables the gate to free-run again (T0). See figure 107a.

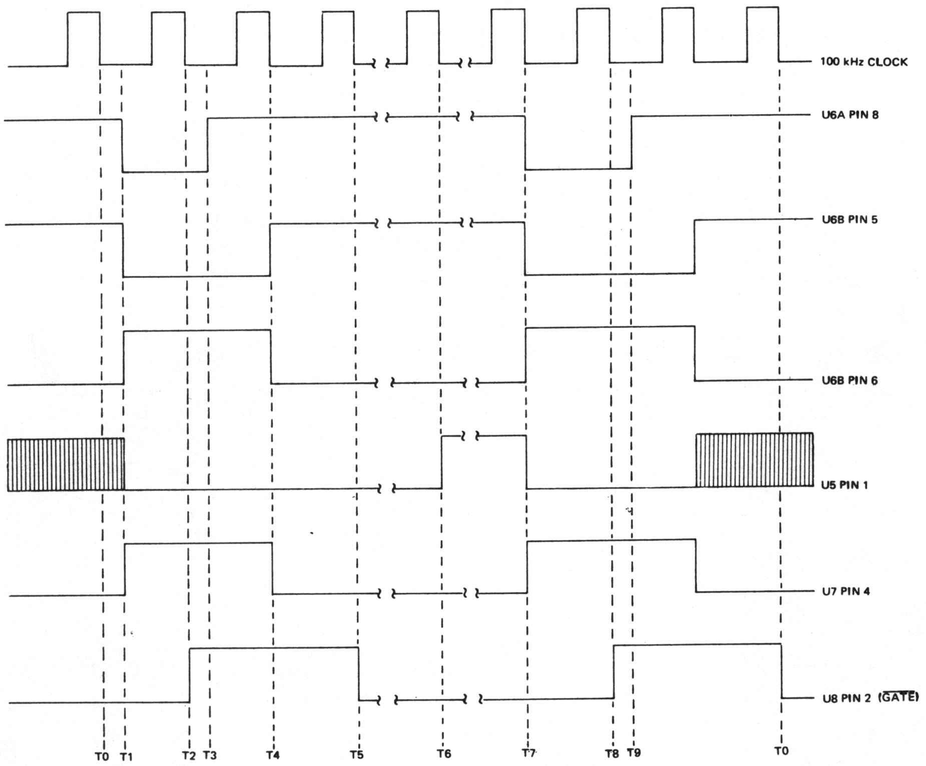


Figure 107a. Gate Generator Timing Diagram

BAND 3 AMPLITUDE DETERMINATION

This circuit consists of three main parts.

- THE POWER METER ZERO DAC is used to automatically zero offsets in the Power Meter. It consists of two 8 bit latching DACs (U3, U4), and a comparator (U14A). All the latching DACs are driven in parallel by shift register U16, with the appropriate DAC being written to by the four write lines (U15, pins 2, 4, 6, 8). The coarse DAC (U3) has a range of ± 200 micro amps, and the fine DAC (U4) has a range of ± 1.5 amps. The Power Meter Zero DAC is adjusted such that, on 1 step U14A is not set, but on the next step U14A is set. This adjusts the input to U14 to 0 volts, nulling any offsets in the power meter curcuit.

- THE POWER METER consists of a 15 dB switchable gain stage (U9), an 8 bit DAC used as a variable attenuator (U10), a 100 mV comparator (U14B), and a latch (half of U17). Two variable attenuators are used, on counters equipped with the option 02 power meter, to provide greater resolution (U10, U12).

  When the detected signal from the microwave converter enters U9 the power meter is first set for maximum gain and minimum attenuation. Next the latch (U17) is reset. If the input to the comparator (U14B) is greater than 100mV, latch U17 will be set. The signal amplitude to the comparator is then reduced, and the process is repeated until latch U17 no longer gets set. The input amplitude can then be calculated from the switch and DAC settings. On counters without the power meter option the amplitude is calculated to a 3dB resolution. On counters with the power meter option the amplitude is calculated to a resolution of 0.1dB.

- The POWER METER PROM (Option 02 only) contains a logic comparator (U21), a 2K X 8 prom (U20), and a bus driver (U19). The logic comparitor is connected to the microprocessor address bus, and is configured to decode the 2K address range from 4000 Hex to 47FF Hex. The comparator output drives the chip select of the Prom, and the bus driver. The prom contains the Power Meter program as well as the power correction factors. Bus driver U19 is used as a buffer for driving the microprocessor data bus.

PERIPHERIAL INTERFACE ADAPTER (PIA)

The Peripherial Interface Adapter (U18) is used as the microprocessor I/O port. It has an address range from 9900 Hex to 9903 Hex. Peripheral Port A is at address 9900, and Peripheral Port B is at address 9902.

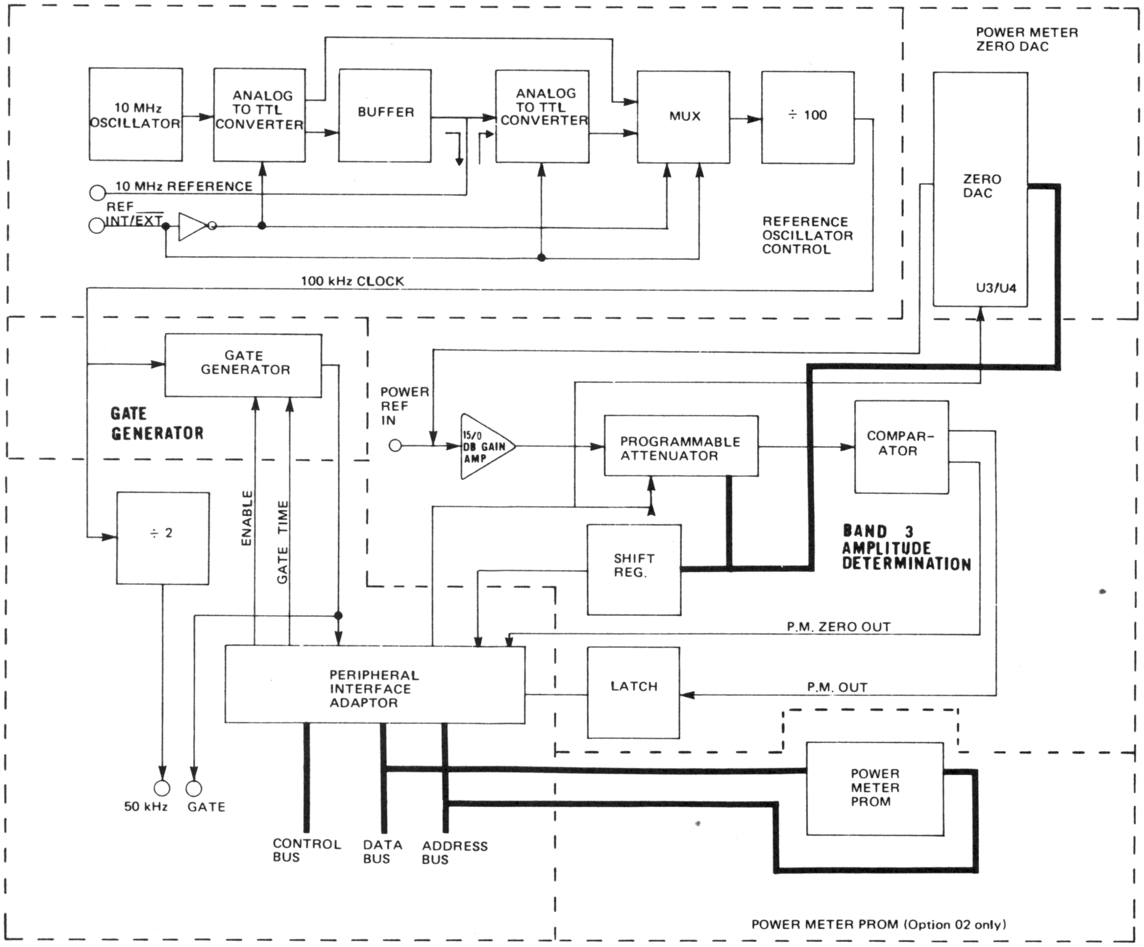

POWER METER ZERO DAC
10 MHz OSCILLATOR
ANALOG TO TTL CONVERTER
BUFFER
ANALOG TO TTL CONVERTER
MUX
÷ 100
ZERO DAC
U3/U4
10 MHz REFERENCE
REF INT/EXT
REFERENCE OSCILLATOR CONTROL
100 kHz CLOCK
GATE GENERATOR
GATE GENERATOR
POWER REF IN
15/0 DB GAIN AMP
PROGRAMMABLE ATTENUATOR
COMPAR-ATOR
÷ 2
ENABLE
GATE TIME
SHIFT REG.
BAND 3 AMPLITUDE DETERMINATION
P.M. ZERO OUT
PERIPHERAL INTERFACE ADAPTOR
LATCH
P.M. OUT
POWER METER PROM
50 kHz
GATE
CONTROL BUS
DATA BUS
ADDRESS BUS
POWER METER PROM (Option 02 only)

Figure 107b. Gate Generator Block Diagram

A107 GATE GENERATOR

2020197 - A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A107	Gate Generator Assy A114 Crystal Osc	2020197 2030002	1 Ref	EIP	
C1	Cer, .01μF, 20%, 100V	2150003	15	TG - S10	72982
C2	C1				
C3	Tant, 33μF, 20%, 10V	2300015	4	TAPA33M10	14433
C4 thru C7	C1				
C8	Mica, 22pF, 5%, 500V	2260017	1	CD10ED220J03	72136
C9	Tant, 1μF, 20%, 35V	2300008	1	TAPA 1.0M35	14433
C10	Mica, 33pF, 5%, 500V	2260021	2	CD10ED330J03	72136
C11	Mica, 100pF, 5%, 500V	2260034	1	CD10FD101J03	72136
C12	C10				
C13 thru C15	C1				
C16	Tant, 10μF, 20%, 25V	2300029	2	DF106M25S	NEC
C17	C1				
C18	C3				
C19	C3				
C20	C1				
C21	C1				
C22	C3				
C23	C1				
C24	C1				
C25	C16				
C26	C1				
CR1	Hot Carrier	2710004	1	FH1100	07263
CR2	Hot Carrier	2710006	1	5002-2800	HP
CR3	CR1 - Option only				
CR4	Zener, 6.2V	2700817	1	IN827	
R1	Comp, 1K, 5%, 1/4W	4010102	2	RC07GF102J	81349
R2	Comp, 200, 5%, 1/4W	4010201	2	RC07GF201J	81349
R3	Comp, 620, 5%, 1/4W	4010621	2	RC07GF621-J	81349
R4	Comp, 2.2K, 5%, 1/4W	4010222	2	RC07GF222J	81349
R5	Comp, 220, 5%, 1/4W	4010221	2	RC07GF221J	81349
R6	Comp, 510, 5%, 1/4W	4010511	2	RC07GF511J	81349
R7	R2				
R8	Comp, 27, 5%, 1/4W	4010270	1	RC07GF270J	81349
R8	Comp, 27, 5%, 1/4W	4010270	1	RC07GF270J	81349
R9	Comp, 300, 5%, 1/4W	4010301	1	RC07GF301J	81349
R10	Comp, 4.7K, 5%, 1/4W	4010472	6	RC07GF472J	81349
R11	R1				
R12	Comp, 390, 5%, 1/4W	4010391	1	RC07GF391J	81349
R13	R10				
R14	R4				
R15	R5				
R16	R6				
R17	R3				
R18	Met Ox, 5.6K, 2%, 1/4W	4130562	1	C4/2%/5.6K	24546
R19	Met Ox, 3.3K, 2%, 1/4W	4130332	1	C4/2%/3.3K	24546
R20	Met Ox, 27, 2%, 1/4W	4130270	1	04/1%/27	24546
R21	Comp, 2.7K, 5%, 1/4W	4010272	1	RC07GF272J	81349
R22	R10				
R23	R10				
R24	Comp, 1.5K, 5%, 1/4W	4010152	2	RC07GF152J	81349

A107 GATE GENERATOR continued

2020197 - A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R25	R24				
R26	Comp, 1.6K, 5%, 1/4W	4010162	1	RC07GF162J	81349
R27	Met Ox, 30K, 2%, 1/4W	4130303	1	C4/2%/30K	24546
R28	Met Ox, 39K, 2%, 1/4W	4130393	1	C4/2%/39K	24546
R29	Prec, 1.69K, 1%, 1/10W	4051691	1	RN55C1691F	81349
R30	Prec, 1.82K, 1%, 1/10W	4051821	1	RN55C1821F	81349
R31	Prec, 57.6K, 1%, 1/10W	4055762	1	RN55C5762F	81349
R32	Comp, 36K, 5%, 1/4W	4010363	1	RC07GF363F	81349
R33	Comp, 15K, 5%, 1/4W	4010153	1	RC07GF153F	81349
R34	Met Ox, 750, 2%, 1/4W	4130751	1	C4/2%/750	24546
R35	Prec, 6.19K, 1%, 1/8W	4056191	1	RN55C6191F	81349
R36	Prec, 100, 1%, 1/8W	4051000	1	RN55C1000F	81349
R37	R10				
R38	R10				
R39	Met Ox, 10K, 2%, 1/4W	4130103	2	C4/02/10K	24546
R40	R39				
RN1	Network, 6.8K	4170005	1	764-1-R6.8K	80740
Q1	NPN - General Purpose	4704124	4	2N4124	
Q2	PNP - General Purpose	4704126	3	2N4126	
Q3	Q1				
Q4	Q2				
Q5	Q1				
Q6	Q2				
Q7	Q1				
Q8	DMOS, FET SW	4710031	1	SD215	18324
U1	Quad Schmitt NAND	3084132	1	SN4LS132	01295
U2	Dual Decade Counter	3084490	1	SN74LS490N	01295
U3	8 Bit DAC	3057524	3	AD7524JN	
U4	U3				
U5	Digital P Chan. MOS Divider	3035009	1	MK5009P	
U6	D Type Pos Flip-flop	3087474	2	SN74LS74N	01295
U7	Quad 21NP NOR Gate	3087402	1	SN74LS02N	01295
U8	Digital Dal D Flip-flop	3110131	1	MC10131L	04713
U9	Dual Low Noise Op Amp	3045532	1	NE5534N	
U10	8 Bit DAC (Option 02 only)	3057525	2	AD7524LN	
U10	U3				
U11	Op Amplifier	3040308	2	LM308AN	27014
U12	U10 (Option 02 only)				
U13	U11				
U14	Comparator	3050393	1	LM393N	27014
U15	Hex Buffer/Driver	3007407	1	DM7407N	27014
U16	Dual 4 Bit Static S/R	3034015	1	MC14015B	04713
U17	U6				
U18	Periph. Interface Adaptor	3085820	1	MC6821	01295
U19	Oct. Buffer) Option	3084244	1	SN74LS244	01295
U20	Power Meter PROM) 02 (-08)	6400001	1	MCM2716	04713
U21	6 Bit Comparator) Only				
U22	Quad Dual Flip-flop	3084175	1	SN74LS175	01295
U23	Op Amp/Lin	3040741	1	LM741CN	27014

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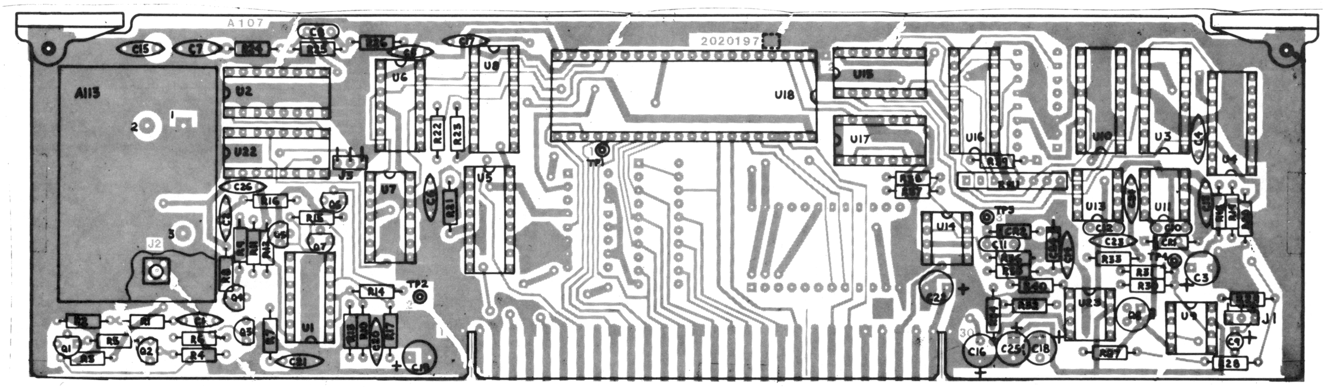
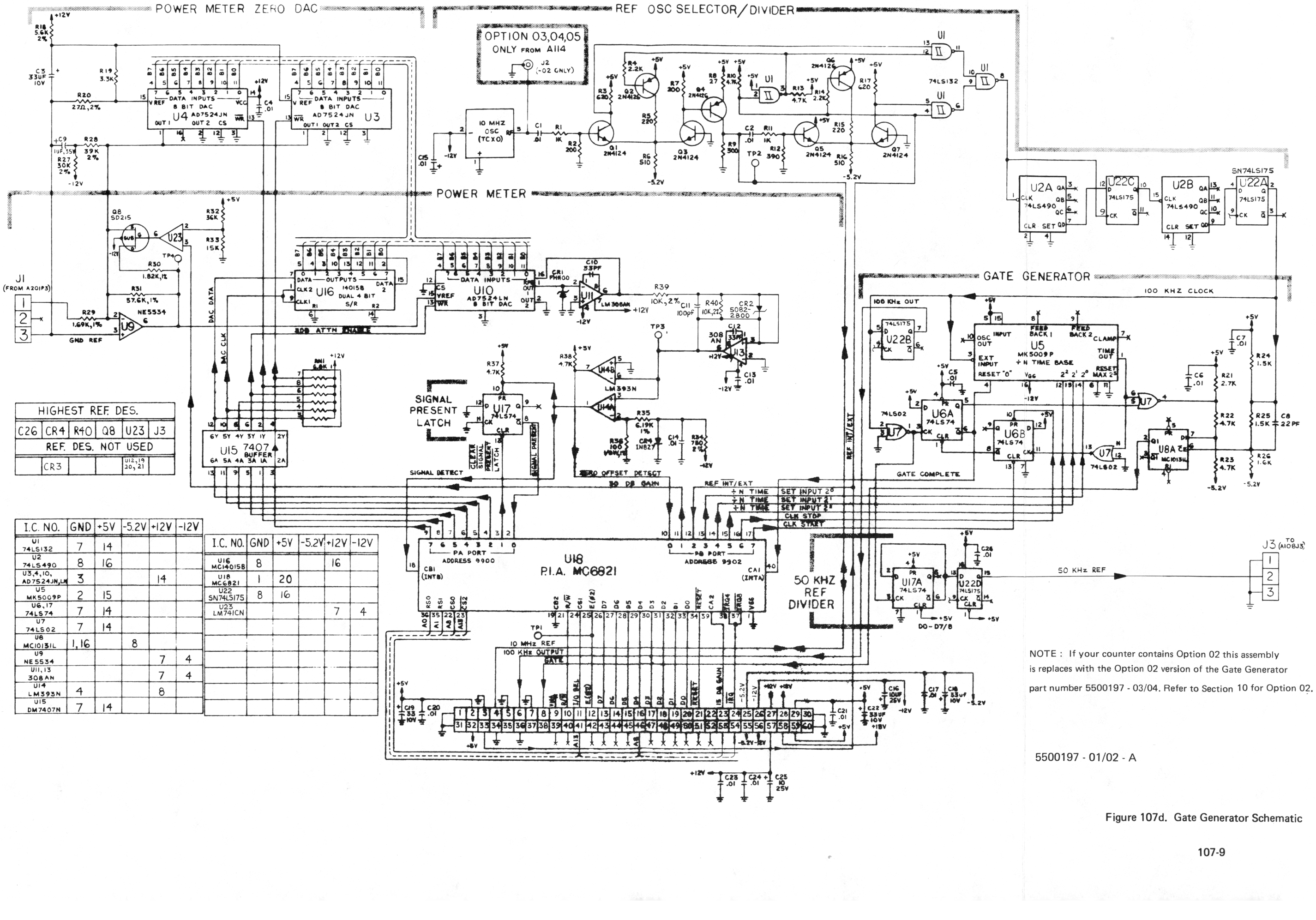

A107
2020197
A113
U2
U22
U6
U8
U18
U15
U17
U16
U10
U3
U4
U7
U5
U14
U13
U11
U1
U23
U9
J1
J2
J3
TP1
TP2
TP3
TP4
C15
C7
C26
C21
C16
C25
C18
C3
R14
R15
R16
R22
R23
R21
R33
R37
R28
Q1
Q2

2020197 - 01/02 - A

Figure 107c. Gate Generator Component Locator

NOTE : If the counter contains Option 02 this board is replaced with the 2020197 - 03/04. Refer to Section 10, Option 02 for the -03/04 version of this assembly.


POWER METER ZERO DAC
REF OSC SELECTOR/DIVIDER
OPTION 03,04,05 ONLY FROM A114
10 MHZ OSC (TCXO)
POWER METER
GATE GENERATOR
SIGNAL PRESENT LATCH
50 KHZ REF DIVIDER
U18 P.I.A. MC6821
J1 (FROM A201P3)
J3 (TO A10BJ3)
50 KHz REF
100 KHZ CLOCK
GATE COMPLETE
SIGNAL DETECT
ZERO OFFSET DETECT
30 DB GAIN
REF INT/EXT
DAC DATA
DAC CLK
30B ATTN ENABLE

HIGHEST REF. DES.					
C26	CR4	R40	Q8	U23	J3
REF. DES. NOT USED					
	CR3			U12,19 20,21	

I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U1 74LS132	7	14			
U2 74LS490	8	16			
U3,4,10, AD7524JN,LN	3			14	
U5 MK5009P	2	15			
U6,17 74LS74	7	14			
U7 74LS02	7	14			
U8 MC10131L	1,16		8		
U9 NE5534				7	4
U11,13 308AN				7	4
U14 LM393N	4			8	
U15 DM7407N	7	14			

I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U16 MC14015B	8			16	
U18 MC6821	1	20			
U22 SN74LS175	8	16			
U23 LM741CN				7	4

NOTE : If your counter contains Option 02 this assembly is replaces with the Option 02 version of the Gate Generator part number 5500197 - 03/04. Refer to Section 10 for Option 02.

5500197 - 01/02 - A

Figure 107d. Gate Generator Schematic

A108
CONVERTER CONTROL
(2020198)

The Converter Control provides a precise YIG tuning current which is controlled by the microprocessor via PIA U4. It will also phase lock the VCO (A201A) in the Microwave Converter (A203) to a selected harmonic of a 50kHz reference signal so that it will provide a synthesized LO. The converter control assembly also permits the microprocessor to control the LO power amplifier and provide the microprocessor input for the IF Threshold signal.

FREQUENCY CONTROL DAC and YIG DRIVER

The yig tuning current is supplied by the yig driver (U3, Q1, Q2, & Q3) which is controlled by the DAC. The DAC is composed of a 12 bit monolithic DAC (U1), summing amplifier (U2) and resistors (R2, R3, R6, & R7) to provide a total resolution of 14 bits. R4 and R5 are pull up resistors for PA ports 0 and 1 of the PIA (U4) which directly drive the 2 least significant bits of the DAC. A change in the least significant bit of the DAC corresponds to a yig frequency change of 2MHz. A voltage analog of yig current appears across R19, and is compared to the DAC output at the summing junction of U3, with resistors R9 and R17.

The slope of yig current vs DAC voltage is adjustable using R10, and the offset is adjusted using R13.

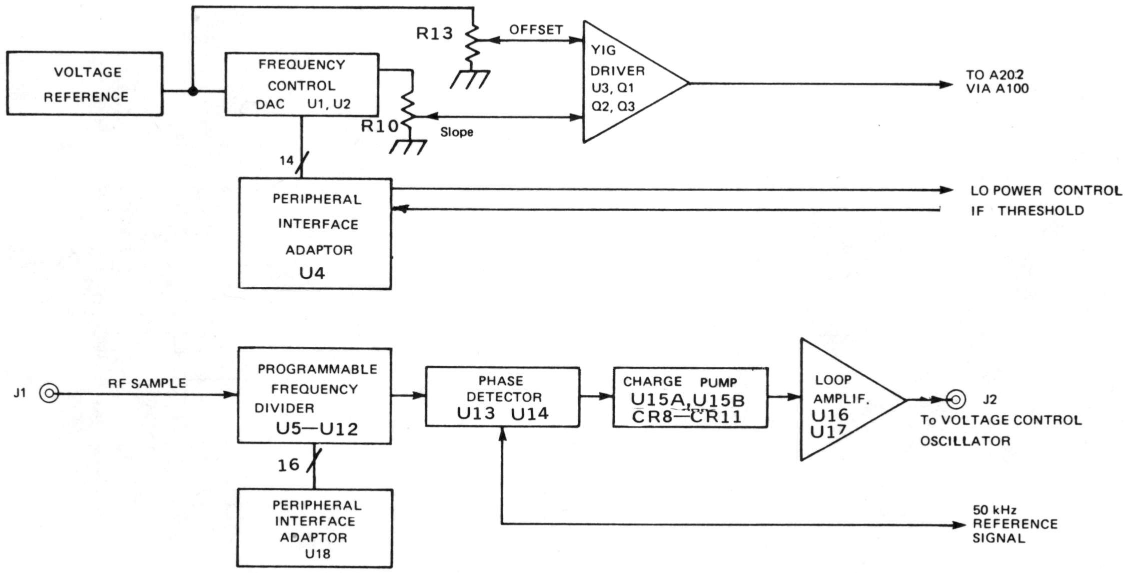

VOLTAGE REFERENCE
FREQUENCY CONTROL DAC U1, U2
R13
OFFSET
YIG DRIVER U3, Q1 Q2, Q3
TO A202 VIA A100
R10
Slope
14
PERIPHERAL INTERFACE ADAPTOR U4
LO POWER CONTROL
IF THRESHOLD
J1
RF SAMPLE
PROGRAMMABLE FREQUENCY DIVIDER U5—U12
PHASE DETECTOR U13 U14
CHARGE PUMP U15A, U15B CR8—CR11
LOOP AMPLIF. U16 U17
J2
To VOLTAGE CONTROL OSCILLATOR
16
PERIPHERAL INTERFACE ADAPTOR U18
50 kHz REFERENCE SIGNAL

Figure 108a. Converter Control Block Diagram

VCO CONTROL

The VCO control circuitry and the VCO (A201A) form a phase lock loop frequency synthesizer. The synthesizer frequency range is 370MHz to 500MHz.

An output signal from the VCO (A201A), via a buffer amplifier on the Band 2 Converter (A109), is applied to the programmable frequency divider (U5 thru U12). The frequency divider is programmed by the microprocessor (A105) via PIA U18. The output of the frequency divider is compared to the 50kHz reference signal from the gate generator (A107) by the phase detector (U13, U14). A phase difference between the divided down VCO and the 50 kHz reference will result in an output from the phase detector. The phase detector has two output ports, a pump-up port and a pump-down port. Pump down is U14 pin 2. It is normally high, and goes low to reduce the VCO frequency. Pump-up is U13 pin 3. It is normally low, and goes high to increase the VCO frequency.

The outputs of the phase detector go to the charge pump, which converts them to a single tri-state output. The charge pump output is open with no pump command, sources about 2 mA with pump down, and sinks about 2 mA with pump up. The output of the charge pump is connected to the input of the loop amplifier (U16, U17). The loop amplifier provides the proper gain and filtering to achieve the desired loop response. The output of the loop amplifier is the VCO tuning voltage. A sample of the tuning voltage is fed back to control the charge pump in such a manner that the loop bandwidth is held fairly constant over the tuning range of the synthesizer.

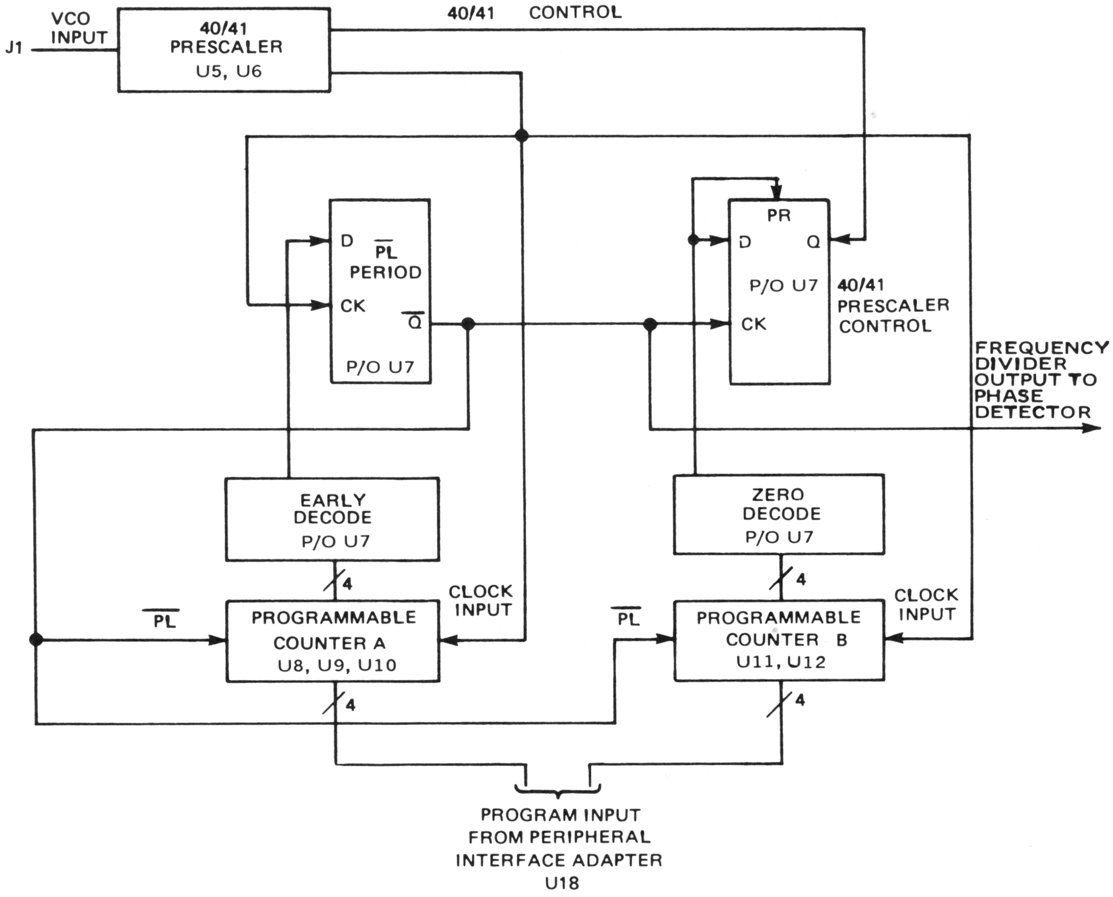

VCO INPUT
J1
40/41 PRESCALER U5, U6
40/41 CONTROL
D
$\overline{PL}$ PERIOD
CK
$\overline{Q}$
P/O U7
PR
D
Q
P/O U7
CK
40/41 PRESCALER CONTROL
FREQUENCY DIVIDER OUTPUT TO PHASE DETECTOR
EARLY DECODE P/O U7
ZERO DECODE P/O U7
4
4
CLOCK INPUT
CLOCK INPUT
$\overline{PL}$
$\overline{PL}$
PROGRAMMABLE COUNTER A U8, U9, U10
PROGRAMMABLE COUNTER B U11, U12
4
4
PROGRAM INPUT FROM PERIPHERAL INTERFACE ADAPTER U18

Figure 108b. Programmable Frequency Divider Block Diagram

PROGRAMMABLE FREQUENCY DIVIDER

The programmable frequency divider uses a two modulus (divide number) prescaler (U5, U6) and two programmable counters (A & B). The prescaler is used to divide the VCO frequency down to a lower frequency which can be handled by low power schottky TTL programmable counters. The two modulus prescaler permits prescaling without loss of resolution. At the start of the programmable frequency divider cycle, the prescaler is set to divide by the larger modulus (41), and both programmable counters have been loaded with their respective program numbers from the PIA (U18). The programmable counters each decrement 1 count for each output pulse from the prescaler. When programmable counter B (U11, U12) reaches the count of zero the 40/41 control flip-flop (part of U7) changes state and causes the prescaler to divide by the lower modulus (40). When programmable counter A reaches the count of 2 the D input of the PL period flip-flop (part of U7) goes high, so that on the count of 1 the flip-flop changes state, which causes both programmable counters to be reloaded with their respective program numbers and the 40/41 control flip-flop to reset (prescaler in ÷ 41 state). The very next count causes the PL period flip-flop to reset, starting the programmable frequency divider cycle over again. The equation for the divide ratio of the programmable frequency divider N_d is:

$$N_d = 40\,(N_{\text{counter A}}) + N_{\text{counter B}}$$

with the condition that:

$$N_{\text{counter B}} \text{ must not exceed } N_{\text{counter A}}$$

The weighting of the command bits is:

U18 P_1 – 400MHz
U8 P_0 – 200MHz
U9 P_3 – 160MHz
U9 P_2 – 80MHz
U9 P_1 – 40MHz
U9 P_0 – 20MHz
U10 P_3 – 16MHz
U10 P_2 – 8 MHz

U10 P_1 – 4MHz
U10 P_0 – 2MHz
U11 P_3 – 1.6MHz
U11 P_2 – 0.8MHz
U11 P_1 – 0.4MHz
U11 P_0 – 0.2MHz
U12 P_1 – 100KHz
U12 P_0 – 50KHz

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A108 CONVERTER CONTROL

2020198 - A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A108	Converter Control Assy	2020198	1	EIP	
C1	Cer, .01μF, 20%, 100V	2150003	14	TG - S10	56289
C2	Mono, .022μF, 15%, 50V	2350027	2	2130X7R050R223K	26654
C3	C1				
C4	Cer, .005μF, 20%, 100V	2150008	1	TG - D50	56289
C5	Tant, 1μF, 10%, 35V	2300008	3	TAG20 - 1/35V	14433
C6	C5				
C7	Cer, .001μF, 20%, 1KV	2150001	4	SGA - D10	56289
C8	C7				
C9	C7				
C10	C7				
C11	C1				
C12	C1				
C13	C1				
C14	Not Used				
C15	Not Used				
C16	C1				
C17	C1				
C18	C1				
C19	C1				
C20	C1				
C21	Mono, 330pF, 10%, 100V	2260054	1	SR211A331KAA	AVX
C22	Mica, 82pF, %, 500V	2260032	1	CD10ED820J03	72136
C23	C1				
C24	Mono, .1μF, 10%, 50V	2260052	1	RC50104KB	GA
C25	C1				
C26	Mono, 2200pF, 5%, 100V	2260050	1	SR211A222JAA	AVX
C27	Mono, 560pF, 5%, 100V	2260053	2	SR211A561KAA	AVX
C28	C27				
C29	C2				
C30	C1				
C31	Tant, 2.2μF, %, 16V	2300012	1	TAPA 2.2M16	14433
C32	Tant, .47μF, %, 35V	2300005	1	TAPA .47M35	14433
C33	Tant, .10μF, %, 35V	2300020	1	TAPA .10M35	14433
C34	C1				
C35	Tant, 33μF, %, 10V	2300015	2	TAPA 33M10	14433
C36	C35				
C37	C5				
C38	Tant, 10μF, %, 25V	2300029	2	DF106M25S	72136
C39	C38				
CR1	Zener, 6.2V	2700827	1	1N827	07263
CR2	Hot Carrier	2710004	1	FH1100	07263
CR3	General Purpose	2704154	12	1N4154	07263
CR4	Zener, 51V	2704757	1	1N4757	07263
CR5	Rectifier	2704001	1	1N4001	07263
CR6 thru CR16	CR3				
CR17	Zener, 4.7V	2705230	1	1N5230	07263
J1	Mini Jack	2610038	2	S1 - 451 - 0000	98291
J2	J1				
J3	Right angle, 3 pin	2620132	1	22 - 05 - 2031	0000A
Q1	NPN, General Purpose	4704124	1	2N4124	04713
Q2	PNP, Amplifier	4710018	1	MPSLS1	04713
Q3	PNP	4710009	1	MJE350	04713

A108 CONVERTER CONTROL continued

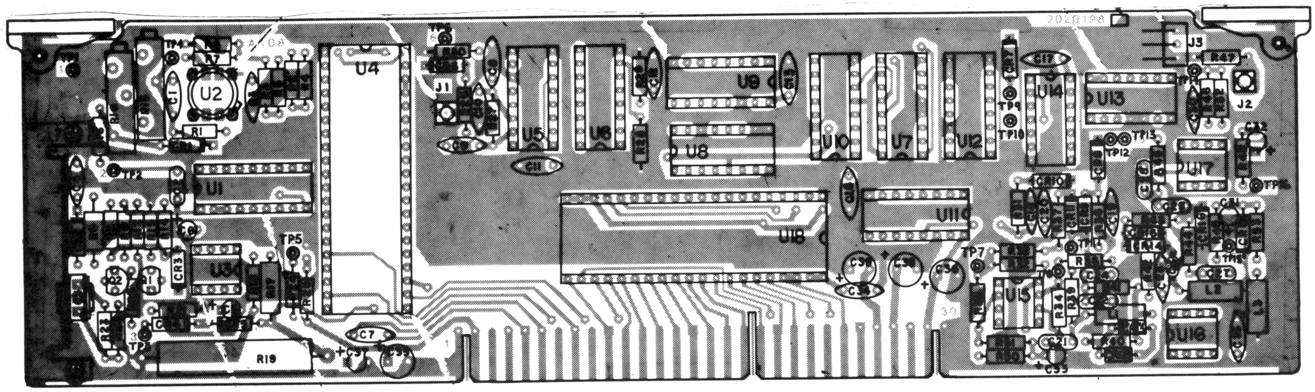
2020198 - A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R1	Comp, 750, 5%, 1/4W	4010751	2	RC07GF751J	81349
R2	Comp, 82K, 5%, 1/4W	4010823	1	RC07GF823J	81349
R3	Comp, 160K, 5%, 1/4W	4010164	1	RC07GF164J	81349
R4	Comp, 10K, 5%, 1/4W	4010103	3	RC07GF103J	81349
R5	R4				
R6	Comp, 820K, 5%, 1/4W	4010824	1	RC07GF824J	81349
R7	Comp, 1K, 5%, 1/4W	4010102	6	RC07GF102J	81349
R8	Comp, 5.1M, 5%, 1/4W	4010515	1	RC07GF515J	81349
R9	Prec, 8.45K, 1%, W	4120019	1	VAR - Y10C - 6 - 1%	ACI
R10	Variable, Cer. MT, 20K	4280011	2	89PR - 20K	
R11	Prec, 49.9K, 1%, 1/4W	4054992	1	RN55C4992F	81349
R12	Met Ox, 10K, 2%, 1/4W	4130103	2	C4/2%/10K	24546
R13	R10				
R14	Prec, 1 meg, 1%, 1/10W	4051004	1	RN55C1004F	81349
R15	R12				
R16	Comp, 4.7K, 5%, 1/4W	4010472	1	RC07GF472J	81349
R17	Prec, 3.01K, 1%, 1/10W	4120020	1	UAR - 1/10 - C6 - 1% - 3.01K	
R18	Met Ox, 1.6K, 2%, 1/4W	4130162	1	C4/2%/1.6K	24546
R19	Wire Wound, 5, 1%, 7W	4110003	1	T7 (10PPM)	
R20	Met Ox, 390, 2%, 1/4W	4130391	2	C4/2%/390	24546
R21	R20				
R22	R7				
R23	R7				
R24	R4				
R25	R7				
R26	Comp, 2.7K, 5%, 1/4W	4010272	1	RC07GF272J	81349
R27	Comp, 51, 5%, 1/4W	4010510	2	RC07GF510J	81349
R28	Comp, 390, 5%, 1/4W	4010391	3	RC07GF391J	81349
R29	R28				
R30	R28				
R31	R7				
R32	Comp, 51K, 5%, 1/4W	4010513	5	RC07GF513J	81349
R33	R32				
R34	R32				
R35	Comp, 100, 5%, 1/4W	4010101	3	RC07GF101J	81349
R36	Comp, 1.1K, 5%, 1/4W	4010112	2	RC07GF112J	81349
R37	R36				
R38	R35				
R39	R27				
R40	Comp, 8.2K, 5%, 1/4W	4010822	1	RC07GF822J	81349
R41	R32				
R42	Comp, 3.3K, 5%, 1/4W	4010332	1	RC07GF332J	81349
R43	Comp, 5.1K, 5%, 1/4W	4010512	1	RC07GF512J	81349
R44	R32				
R45	Comp, 7.5K, 5%, 1/4W	4010752	1	RC07GF752J	81349
R46	R35				
R47	R7				
R48	Comp, 220K, 5%, 1/4W	4010224	1	RC07GF224J	81349
R49	Comp, 1.5M, 5%, 1/4W	4010155	1	FC07GF155J	81349
R50	Comp, 120K, 5%, 1/4W	4010124	1	RC07GF124J	81349
R51	Comp, 43K, 5%, 1/4W	4010433	1	RC07GF433J	81349
R52	Comp, 100K, 5%, 1/4W	4010104	1	RC07GF104J	81349
R53	R1				
TP1 thru TP16	Pin, .04D, Gold	2620032	16	460 - 2970 - 02 - 03	71279

A108 CONVERTER CONTROL continued

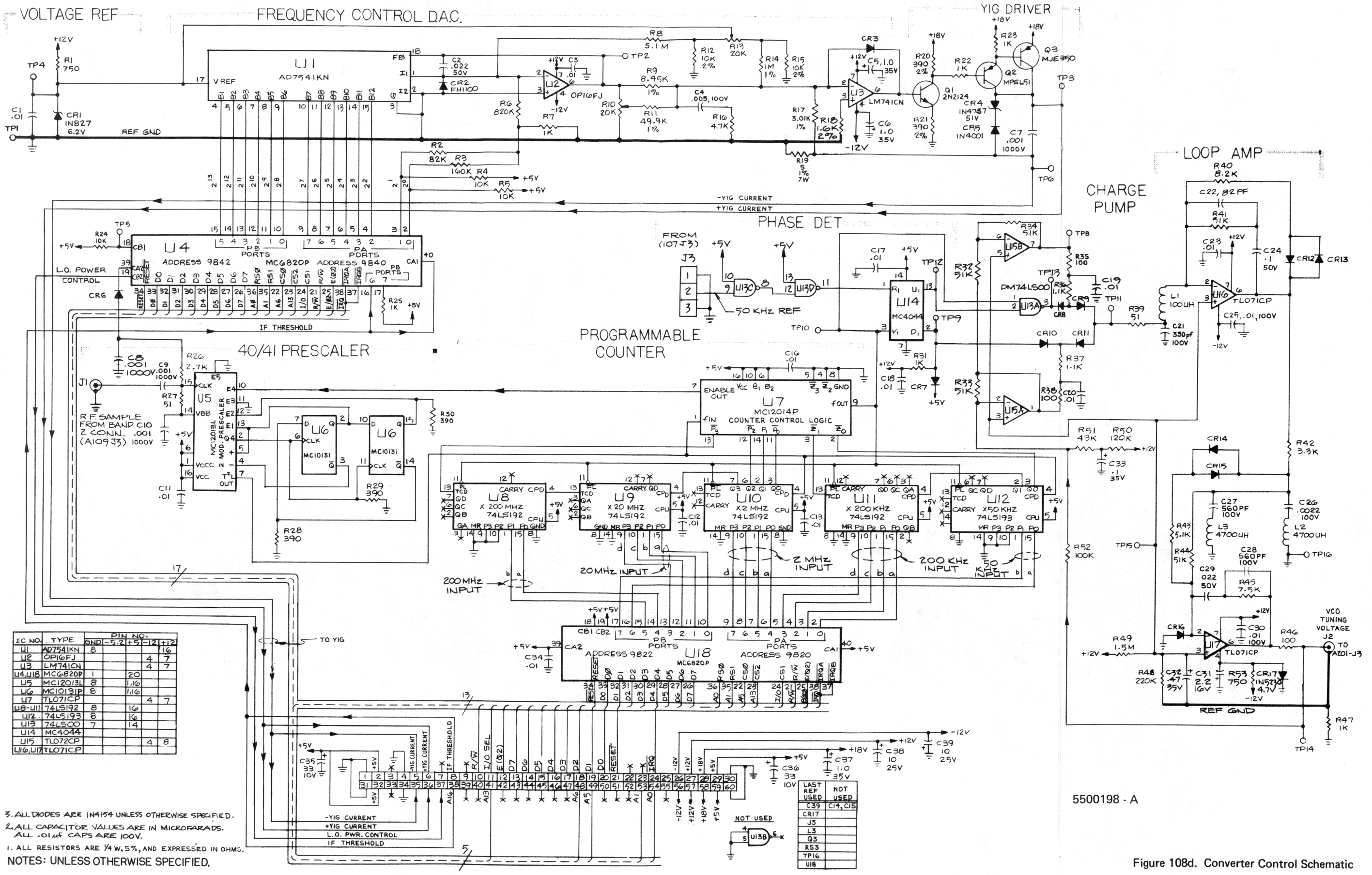
2020198 - A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
U1	12 Bit DAC	3057541	1	AD7541KN	0000X
U2	Prec. J. FET Op Amp	3041016	1	OP16FJ	06665
U3	Op Amp	3040741	1	LM741CN	27014
U4	Peripheral Interface Adaptor	3086820	2	MC6820P	04713
U5	Two-Mod Prescaler	3112013-02	1	MC12013L	04713
U6	Digital Dual "D" Flip-flop	3110131	1	MC10131L	04713
U7	Counter Control Logic	3112014	1	MC12014P	04713
U8 thru U11	UP/DOWN Counter	3084192	4	DM74LS192N	27014
U12	UP/DOWN Counter	3084193	1	DM74LS193N	27014
U13	Quad 2INP NAND	3087400	1	DM74LS00	27014
U14	Phase Freq. Detector	3014044	1	MC4044P	04713
U15	Op Amp, J FET	3040072	1	TL072CP	0000X
U16	Op Amp, J FET	3040071	2	TL071CP	0000X
U17	U16				
U18	U4				
L1	Inductor, 100μH	3520007	1	1537-76	
L2	Inductor, 4700μH	3510017	2	1641-475	
L3	L2				


2020198
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
J1
J2
J3
R1
R7
R19
R47
C7
C11
C17
CR3
L2
TP2
TP4
TP5
TP7
TP9
TP10
TP12
TP13

2020198 - B

Figure 108c. Converter Control Component Locator


VOLTAGE REF
FREQUENCY CONTROL DAC
YIG DRIVER
LOOP AMP
CHARGE PUMP
PHASE DET
PROGRAMMABLE COUNTER
40/41 PRESCALER
U1 AD7541KN
U2 OP16FJ
U3 LM741CN
U4 MC6820P ADDRESS 9842 ADDRESS 9840
U5 MC12013L
U6 MC10131
U7 MC12014P COUNTER CONTROL LOGIC
U8 X 200 MHZ 74LS192
U9 X 20 MHZ 74LS192
U10 X2 MHZ 74LS192
U11 X 200 KHZ 74LS192
U12 X50 KHZ 74LS193
U13 PM74LS00
U14 MC4044
U15 TL072CP
U16 TL071CP
U17 TL071CP
U18 MC6820P ADDRESS 9822 ADDRESS 9820
REF GND
-YIG CURRENT
+YIG CURRENT
L.O. POWER CONTROL
IF THRESHOLD
FROM (107J3)
50 KHz REF
R.F. SAMPLE FROM BAND C10 2 CONN. (A109J3)
200MHz INPUT
20MHz INPUT
2 MHz INPUT
200 KHz INPUT
50 KHz INPUT
TO YIG
VCO TUNING VOLTAGE J2 TO A201-J3
NOT USED

IC NO.	TYPE	PIN NO.				
		GND	-5.2	+5	-12	+12
U1	AD7541KN	8				16
U2	OP16FJ				4	7
U3	LM741CN				4	7
U4,U18	MC6820P	1		20		
U5	MC12013L	8		1,16		
U6	MC10131P	8		1,16		
U7	TL071CP				4	7
U8-U11	74LS192	8		16		
U12	74LS193	8		16		
U13	74LS00	7		14		
U14	MC4044					
U15	TL072CP				4	8
U16,U17	TL071CP					

LAST REF USED	NOT USED
C39	C14, C15
CR17	
J3	
L3	
Q3	
R53	
TP16	
U18	

3. ALL DIODES ARE 1N4154 UNLESS OTHERWISE SPECIFIED.

2. ALL CAPACITOR VALUES ARE IN MICROFARADS. ALL .01uf CAPS ARE 100V.

1. ALL RESISTORS ARE 1/4 W, 5%, AND EXPRESSED IN OHMS.

NOTES: UNLESS OTHERWISE SPECIFIED.

5500198 - A

Figure 108d. Converter Control Schematic

A109
BAND 2 CONVERTER
(2020139)

The Band 2 Converter accepts Band 1 and Band 2 RF signals from the front panel, and local oscillator (LO) signal from the Band 3 Converter (A203). The appropriate signal is selected and processed to produce an IF signal between 10 Hz and 200 MHz. The IF signal output is sent to the Count Chain board (A106), and lock information is routed through the PIA (peripheral interface adapter) U2 to the Microprocessor (A105).

IMPEDANCE CONVERTER

Band 1 input from the front panel enters the converter at J6 and is terminated by R75. The signal is coupled to the input of a field effect transistor (FET) amplifier (Q15) through an RC network (R73, C42). Two limiter diodes (CR4, CR5) protect the FET against large input signals. The FET is a source follower with slightly less than unity gain. The FET drives a buffer amplifier (Q14) which has enough gain to increase the impedance converter overall gain to near unity. A decoupling capacitor (C39) controls the amplifiers low frequency cutoff, and C41 provides high frequency peaking to keep the gain flat to frequencies above 100 MHz.

SIGNAL SELECT

The output of the impedance converter circuit drives one input of the signal select circuitry. Signal selection is made by enabling one of three differential amplifiers, U4A, U4B, or U5A. When Band 1 is selected, a logic high signal on the PIA (U2 pin 2) turns on Q16. Q16 biases on the current source in U4A. This current source generates an 11ma current which is split between the two differential amplifier transistors in U4A. The currents from pins 5 and 6 flow through matched collector loads (R94, L7/R95, L8). R94 and R95 are equal, and are selected for the proper low frequency gain during board alignment. Inductors L7 and L8 provide peaking to give an approximate flat gain through 200MHz. Diodes CR9 and CR10 provide limiting on very strong signals to prevent the next stage from being over driven.

The next stage is a differential amplifier similar to U4A, but it is driven differentially. To generate a single ended output signal, one output of U5B (pin 12) is passed through a current mirror (Q18). The output of the current mirror is then added to the second output of U5B (pin 11) at J5. The load for this stage is a 51 ohm resistor located on the A106 Count Chain board in order to terminate the coax for RF signals. In the quiescent state, the current from Q18 equals the collector current of the differential amplifier U5B, and the output current is zero. When a signal is applied, the current will be unbalanced to generate a signal at the load resistor. To provide frequency compensation of the current mirror, an RC network (R108, C34) is connected between the emitter of Q18 and ground.

BAND 1 LOCK DETECTOR

The output signal at J5 is coupled to detector CR12. Amplifier U6 is a threshold comparator that will produce a logic low signal when the IF output from J5 is more than –6dBm. The output of U6 goes through a resistor divider network to generate a 5V TTL logic signal for the PIA. R90 provides about 1 dB of positive feedback at threshold level to prevent eratic output from the comparator.

ISOLATION AMPLIFIER

The Band 2 input signal enters on J4. This RF signal is terminated in 50 ohms by the combination of R1 and the input impedance of the amplifier. The input signal level is detected by CR1, filtered by C3, and applied to one input of the Band 2 lock detector (U1).

The isolation amplifier is a common base amplifier with a gain of –10 dB. An input signal range of +10 to –20dBm is translated to a 0 to –30dBm range into the mixer so the mixer will be in its linear range for all signal input levels. The amplifier peaks slightly near 1 GHz to overcome an increase in mixer conversion loss at these frequencies.

MIXER OPERATION

The local oscillator (LO) is applied to the IF terminal and the IF is removed from the LO terminal. This swap allows the mixer (MX1) to be unbalanced and act as a low loss attenuator for signals between 10MHz and 200MHz where no mixing is necessary. The mixer has a nominal 400MHz LO for signals between 200MHz and 600MHz; and has a nominal 800MHz LO for signals between 600MHz and 1GHz. A 980MHz LO allows operation with input signals to 1160MHz.

IF AMPLIFIER

The output of the mixer drives an IF amplifier through a 7 section, 200MHz low-pass filter. The IF amplifier is a "feedback pair" amplifier whose gain is stabilized by feedback, to be equal to 24dB. Inductor L6 is used to extend the high frequency response to 200MHz. The 1 pF capacitor (C26) between R34 and R35 is a low pass filter to reduce the 1200 to 1500 MHz LO harmonics that reach the IF amplifier.

BAND 2 LOCK DETECTOR

The IF amplifier output goes to the signal select circuit and to the Band 2 Lock Detector. The Band 2 Lock Detector has a voltage proportional to the IF level on the positive input, and a voltage proportional to the RF signal on the Negative input. The conversion gain from RF input to IF amplifier output is a +6dB for all valid signals, and less than –6dB for all spurious signals. The output of U1 is positive only when a valid IF signal is present. A small offset is added by R12 and R13 to guarantee a non lock condition when no signal is present. Resistor R90 provides about 1dB of positive feedback to prevent eratic output from noise at the point of threshold.

LO BUFFER

The VCO signal from the Band 3 Converter (A201A, J2) enters on J1. The signal goes through a 6 dB attenuator (R111, R112, R114), and a low pass filter (L1, C63, C64 to attenuate high order harmonics), and is terminated by a 51 ohm resistor (R16). Two high input impedance signal splitters (Q2, Q3) get their input signals from R16. Q2 and Q3 operate on the same basic principal. One output is taken from the emitter (acting as an emitter follower) which provides unity gain for the input signal. The AC terminating impedance on the emitter is adjusted to be 50 ohms so the amplifier will act as a unity gain amplifier for the 50 ohm load which terminates the collector when a coax cable is connected. U2 has an additional transformer (T1) in its collector lead to increase the signal output to J3 by about 4 dB.

DIVIDE-BY-TWO

The emitter output of Q3 drives the input of a divide-by-two IC (U3). The impedance is held at 50 ohms by two terminating/biasing resistors (R61, R62). The resistors keep the input bias to U3 below the emitter-coupled logic (ECL) low level (approx. −2.0V). The microprocessor enables self-test by putting a low level signal on pin 5 of the PIA (U2). This turns on Q13, and raises the voltage at U3 pin 7 to the center of an ECL signal (approx. −1.2V). This allows U3 to divide the input signal by two. The output of U3 goes to the signal select circuits.

LO SELECT

The signal from the emitter of Q2 drives the LO select circuitry. The LO provides one (of three) signals to the mixer (MX1). In Band 2A a bias current is generated to unbalance the mixer and allow signals below 190MHz to pass. In Band 2B a 370MHz or 425MHz LO signal is generated that will mix with signals of 200 to 600MHz, and provide the 10 to 200MHz IF signal desired. In Band 2C a 750MHz, 850MHz or 980MHz LO signal is generated to mix with input signals between 600MHz and 1160MHz to provide the desired IF signal.

In Band 2A, the 3ma current to bias mixer MX1 is generated when Q12 is turned on by the PIA, to apply +12V to MX1 through R57. This will allow signals to pass that are less than the cutoff frequency of the low pass filter (200MHz). The LO signal to mixer MX2 from Q2 is not allowed to pass MX2 because of the inherent balance of the mixer. No signal can enter pin 2 of MX2 because Q7 has been saturated, removing bias from buffer Q5, and shunting any RF signals to ground.

When Band 2B is selected, Q12 is turned off thus balancing mixer MX1; Q6 is turned on to unbalance mixer MX2. With MX2 unbalanced, the LO signal from Q2 can pass through MX2 and be amplified by Q10 and Q11, and be applied to mixer MX1.

When Band 2C is selected both Q6 and Q12 are off, and both mixers are balanced. In this mode Q7 is shut off and an LO signal is applied to pin 1 and 2 of MX2. The sum output of MX2 is selected by a DC blocking capacitor (C31). This sum (that is two times the incoming LO frequency) is amplified by Q10 and Q11 and applied to MX1.

The Q10 and Q11 amplifier is a series shunt pair. Q10 applies most of the RF input signal across the emitter resistor R47. This determines the transistor emitter current, which will be the collector current if the output is terminated in a low impedance. Q11 is used as a current-to-voltage converter. The output voltage of this converter is the product of the input current times the feedback resistor (R51). Since the input of this stage is a summing junction, it appears very close to zero ohms to the previous stage, Q10. The voltage gain of the two transistors can be approximated by R51/R47, which is about 3 or 10dB. Since the gain required at 800MHz is slightly greater than required at 400MHz, a low pass matching network (consisting of L2 and C20 peaks the output signal current to MX1 at 800 MHz. The remaining components around Q10 and Q11 are used to bias the transistors. Shunt biasing is used to provide collector bias voltages of 3.4V for Q10, and 4.7V for Q11.

OPTION SELECTION

Provision has been made on this assembly for a set of jumpers that will let the microprocessor know when it has the components required for a 548A (26.5 GHz) counter, and if it has an extended frequency option (Option 06). These jumpers are read by the microprocessor when the counter is turned on, and will select micro code which is applicable only when those options are available. A jumper from E1 to E3 (from pins 8 and 9 on the PIA U2) indicate that this is a 548A counter. A jumper from E2 to E4 indicates that Option 06 (Band 4) has been installed.

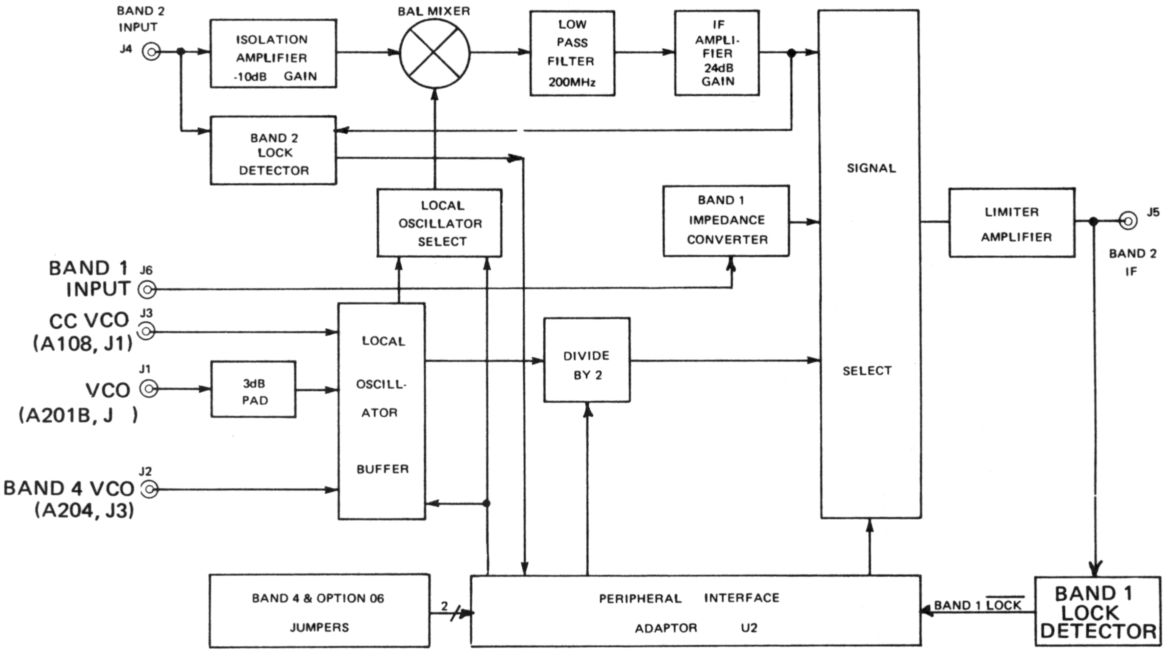

BAND 2 INPUT
J4
ISOLATION AMPLIFIER -10dB GAIN
BAL MIXER
LOW PASS FILTER 200MHz
IF AMPLIFIER 24dB GAIN
BAND 2 LOCK DETECTOR
LOCAL OSCILLATOR SELECT
BAND 1 IMPEDANCE CONVERTER
SIGNAL SELECT
LIMITER AMPLIFIER
J5
BAND 2 IF
BAND 1 J6 INPUT
CC VCO J3 (A108, J1)
J1 VCO (A201B, J)
3dB PAD
LOCAL OSCILLATOR BUFFER
DIVIDE BY 2
J2 BAND 4 VCO (A204, J3)
BAND 4 & OPTION 06 JUMPERS
2
PERIPHERAL INTERFACE ADAPTOR U2
BAND 1 LOCK
BAND 1 LOCK DETECTOR

Figure 109a. Band 2 Converter Block Diagram

A109 BAND 2 CONVERTER

2020139 - L

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A109	Band 2 Converter Assy	2020139	1	EIP	
C1	Cer, .01μF, 10%, 100V	2150014	9	6123X7R103KA100	26654
C2	C1				
C3	Cer, .001μF 10%, 100V	2150015	11	6183X7R102KA100	26654
C4 thru C6	C1				
C7	Mica, 100pF, 5%, 500V	2260034	3	FD101J03	72136
C8	Disc, .001μF, 20%, 1KV	2150001	8	SGA - D10	56289
C9	Disc, .01μF, 20%, 100V	2150003	11	TG - S10	56289
C10	C8				
C11	C8				
C12	C7				
C13	C8				
C14	C7				
C15 thru C18	C3				
C19	C8				
C20	Mica, 1pF, 5%, 500V	2260005	2	CD010C03	56289
C21	Mica, 18pF, 5%, 500V	2260015	3	CD180J03	56289
C22	Mica, 33pF, 5%, 500V	2260021	2	ED330J03	56289
C23	C22				
C24	C21				
C25	C1				
C26	C20				
C27	Not Used				
C28	C1				
C29	C9				
C30	C1				
C31	C3				
C32	C3				
C33	C1				
C34 thru C36	C3				
C37	C9				
C38	C3				
C39	Tant, 100μF, 20%, 6.3V	2300024	1	TAG20 - 47/6.3 - 50	14433
C40	C9				
C41	Mica, 22ρF, 5%, 500V	2660017	1	ED220J03	72136
C42	Mica, 47pF, 5%, 500V	2260004	1	DM10 - 470J	72136
C43	Tant, 33μF,10%, 10V	2300015	6	TAG20 - 33/10 - 50	14433
C44	C9				
C45	C43				
C46	C8				
C47 thru C49	C9				
C50	Tant, 10μF, 20%, 25V	2300029	3	TAG20 - 10/25	14433
C51	C43				
C52	C9				
C53	C9				
C54	C21				
C55	C8				
C56	C8				
C57	C50				

A109 BAND 2 CONVERTER, continued

2020139-L

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
C58	C43				
C59	C9				
C60	C43				
C61	C50				
C62	C43				
C63	Mica, 8pF, 5%, 500V	2660011	2	CD080J03	56289
C64	C63				
CR1	Mix UHF	2710038	2	ND4991	00005
CR2	Not Used				
CR3	CR1				
CR4	General Purpose	2704154	3	1N4154	07263
CR5	CR4				
CR6 thru CR10	Not Used				
CR11	CR4				
CR12	CR1				
L1 thru L5	Part of Board				
L6	Inductor, 0.47 =H	3510006	1	DD - 0.47	99800
L7	L1				
L8	L1				
MX1	Balanced Mixer	2030016	2	TFM-12	
MX2	MX1				
Q1	NPN, RF	4710030	7	BFR-90	04713
Q2	Q1				
Q3	Q1				
Q4	PNP, General Purpose	4704124	1	2N4124	04713
Q5	Q1				
Q6	PPNP, General Purpose	4704126	7	2N4126	04313
Q7	Q1				
Q8	Q1				
Q9	NPN, RF	4710024	2	BFR-90	04713
Q10	Q1				
Q11	Q9				
Q12	Q6				
Q13	Q6				
Q14	NPN, RF	4710023	2	A5T4261	01295
Q15	NN-Channel, JFET	4704416	1	2N4416	04713
Q16	Q6				
Q17	Q6				
Q18	Q14				
Q19	Q6				
Q20	Q6				
R1	Comp, 150, 5%, 1/8 W	4000151	1	RC05GF151J	81349
R2	Met Ox, 75, 2%, 1/4 W	4130750	2	C4/2%/75	24546
R3	Comp, 1.1K, 5%, 1/4 W	4010112	1	RC07GF112J	81349
R4	Comp, 820, 5%, 1/4 W	4010821	3	RC07GF821J	81349
R5	Comp, 33, 5%, 1/8 W	4000330	1	RC05GF330J	81349
R6	Comp, 51, 5%, 1/8 W	4000510	1	RC05GF510J	81349
R7	Comp, 10K, 5%, 1/4 W	4010103	3	RC07GF103J	81349
R8	Met Ox, 8.2K, 2%, 1/4 W	4130822	2	C4/2%/8.2K	81349
R9	Met Ox, 30K, 2%, 1/4 W	4130303	1	C4/2%/30K	24546
R10	Met Ox, 43K, 2%, 1/4 W	4130433	2	C4/2%/43K	24546
R11	Comp, 43K, 5%, 1/4 W	4010433	1	RC07GF433J	81349
R12	Met Ox, S.A.T., Nom, 15K	4130999	1	C4/2%/15K	24546
R13	Met Ox, 12, 2%, 1/4 W	4130120	1	C4/2%/12	24546

A109 BAND 2 CONVERTER, continued

2020139-L

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R14	Comp, 36, 5%, 1/4 W	4010360	1	RC07GF36J	81349
R15	Comp, 11, 5%, 1/4 W	4010110	2	RC07GF110J	81349
R16	Met Ox, 51, 2%, 1/4 W	4130510	2	C4/2%/51	24546
R17	Comp, 1K, 5%, 1/4 W	4010102	5	RC07GF102J	81349
R18	R4				
R19	R15				
R20	R17				
R21	Comp, 220, 5%, 1/4 W	4010221	2	RC07GF221J	81349
R22	Comp, 20K, 5%, 1/4 W	4010203	1	RC07GF203J	81349
R23	R4				
R24	Comp, 10, 5%, 1/8 W	4010100	11	RC07GF100J	81349
R25	Met Ox, 750, 2%, 1/4 W	4130751	2	C4/2%/750	24546
R26	Comp, 11k, 5%, 1/4 W	4010113	3	RC07GF113J	81349
R27	Met Ox, 4.7K, 2%, 1/4 W	4130472	1	C4/2%/4.7K	24546
R28	Met Ox, 33, 2%, 1/4 W	4130330	2	C4/2%/33	24546
R29	Comp, 4.7K, 5%, 1/4 W	4010472	2	RC07GF472J	81349
R30	R26				
R31	Comp, 8.2K, 5%, 1/4 W	4010822	2	RC07GF822J	81349
R32	R7				
R33	R7				
R34	Met Ox, 27, 2%, 1/4 W	4130270	1	C4/2%/27	24546
R35	Met Ox, 24, 2%, 1/4 W	4130240	1	C4/2%/24	24546
R36	R24				
R37	Comp, 10, 5%, 1/8 W	4000100	1	RC05GF100J	81349
R38	R17				
R39	Met Ox, 1K, 2%, 1/4W	4130102	1	C4/2%/1K	24546
R40	Met Ox, 820, 2%, 1/4 W	4130821	2	C4/2%/820	24546
R41	R24				
R42	R16				
R43	R24				
R44	Comp, 910, 5%, 1/4 W	4010911	1	RC07GF911J	81349
R45	Comp, 3.9K, 5%, 1/4 W	4010392	2	RC07GF392J	81349
R46	Comp, 27K, 5%, 1/4 W	4010273	1	RC07GF273J	81349
R47	R28				
R48	Comp, 3.3K, 5%, 1/4 W	4010332	1	RC07GF332J	81349
R49	Comp, 390, 5%, 1/4 W	4010391	1	RC07GF391J	81349
R50	Comp, 13K, 5%, 1/4 W	4010133	1	RC07GF133J	81349
R51	Met Ox, 120, 2%, 1/4 W	4130121	1	C4/2%/120	24546
R52	R24				
R53	R31				
R54	R26				
R55	R25				
R56	R24				
R57	Met Ox, 3.9K, 2%, 1/4 W	4130392	4	C4/2%/3.9K	24546
R58	R17				
R59	R45				
R60	Met Ox, 560, 2%, 1/4 W	4130561	1	C4/2%/561	24546
R61	Met Ox, 82, 2%, 1/4 W	4130820	1	C4/2%/82	24546
R62	Met Ox, 130, 2%, 1/4 W	4130131	2	C4/2%/130	24546
R63	Comp, 510, 5%, 1/4 W	4010511	1	RC07GF511J	81349
R64	Comp, 51, 5%, 1/4 W	4010510	2	RC07GF510J	81349
R65	Comp, 200, 5%, 1/4 W	4010201	1	RC07GF201J	81349
R66	Comp, 160K, 5%, 1/4 W	4010164	1	RC07GF160K	81349
R67	Met Ox, 1.8K, 2%, 1/4 W	4130182	1	C4/2%/1.8K	24546
R68	R24				
R69	Met Ox, 510, 2%, 1/4 W	4130511	2	C4/2%/510	24546
R70	Met Ox, S.A.T. Nom 1.2K	4130999	1	C4/2%/1.2K	24546
R71	R29				
R72	R24				

A109 BAND 2 CONVERTER, continued

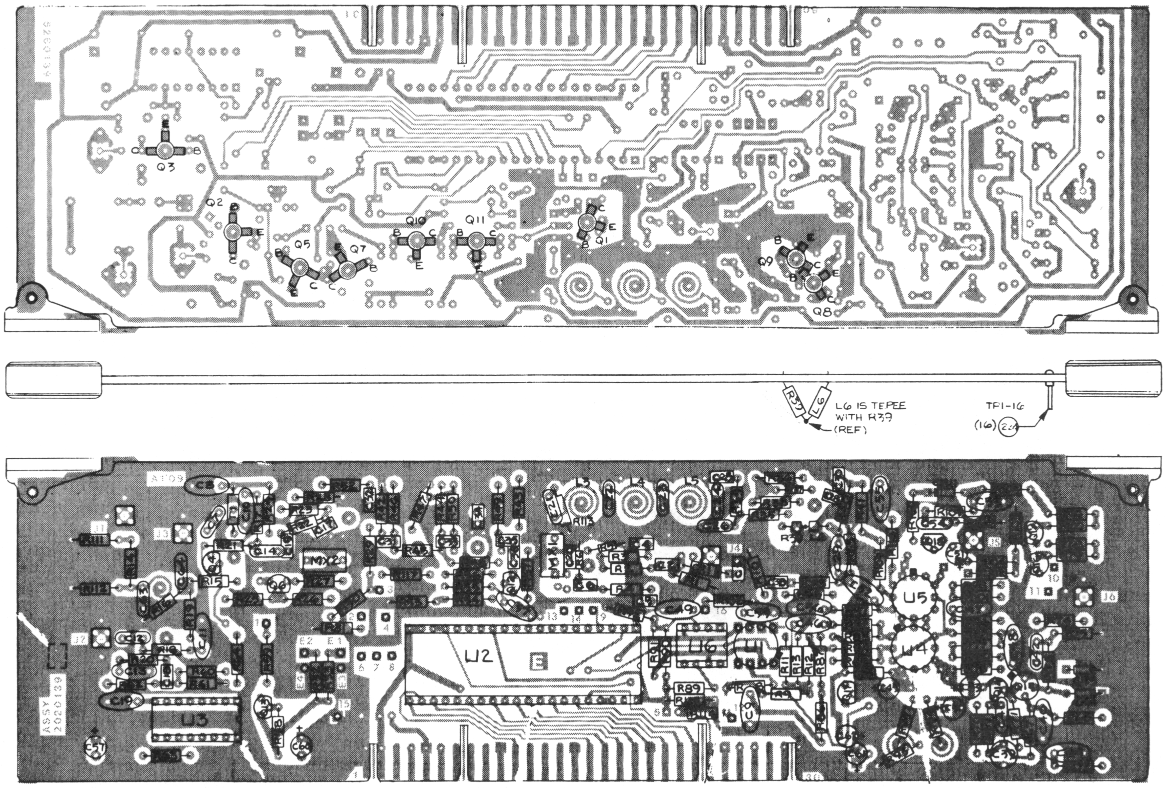
2020139-L

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R73	Comp, 1M, 5%, 1/4 W	4010105	2	RC07GF105J	81349
R74	R64				
R75	R73				
R76	Met Ox, 2.2K, 2%, 1/4 W	4130222	3	C4/2%/2.2K	24546
R77	R57				
R78	Comp, 5.6K, 5%, 1/4 W	4010562	1	RC07GF562J	81349
R79	Comp, 3.6K, 5%, 1/4 W	4010362	3	RC07GF362J	81349
R80	Met Ox, 7.5K, 2%, 1/4 W	4130752	3	C4/2%/7.5K	24546
R81	R76				
R82	R24				
R83	Met Ox, 200, 2%, 1/4 W	4130201	3	C4/2%/200	24546
R84	R57				
R85	Met Ox, 330, 2%, 1/4 W	4130331	1	C4/2%/330	24546
R86	Comp, 6.8K, 5%, 1/4 W	4010682	2	RC07GF682J	81349
R87	R79				
R88	R80				
R89	R8				
R90	Comp, 75K, 5%, 1/4 W	4010753	1	RC07GF753J	81349
R91	Met Ox, 33K, 2%, 1/4 W	4130333	1	C4/2%/33K	24546
R92	Met Ox, 160, 2%, 1/4 W	4130161	1	C4/2%/161	24546
R93	R21				
R94	Met Ox, S.A.T.	4130999	2	C4/2%/12	
R95	R94				
R96	R83				
R97	R83				
R98	R57				
R99	R86				
R100	R79				
R101	R80				
R102	R10				
R103	R76				
R104	Comp, 180, 5%, 1/4 W	4010181	1	RC07GF181J	81349
R105	R24				
R106	Met Ox, 91, 2%, 1/4 W	4130910	1	C4/2%/91	24546
R107	R62				
R108	R24				
R109	R69				
R110	R17				
R111	Comp, 160, 5%, 1/4 W	4010161	2	RC07GF161J	81349
R112	R111				
R113	Met Ox, 20, 2%	4130200	1	C4/2%/9.1K	24546
R114	Met Ox, 2K, 2%, 1/4 W	4130202	1	C4/2/2K	24546
R115	R114				
R116	Met Ox, 9.1K, 2%, 1/4 W	4130912	1	C4/2%/9.1K	24546
R1117	R116				
R118	Comp, 300Ω %, 1/4 W	4010301	1	RC07GF301J	
R19	Comp, 3.9K, %, 1/4 W	4010392	3	RC07GF392J	
R20	Comp, 820Ω %, 1/4 W	4010821	4	RC07GF821J	

A109 BAND 2 CONVERTER, continued

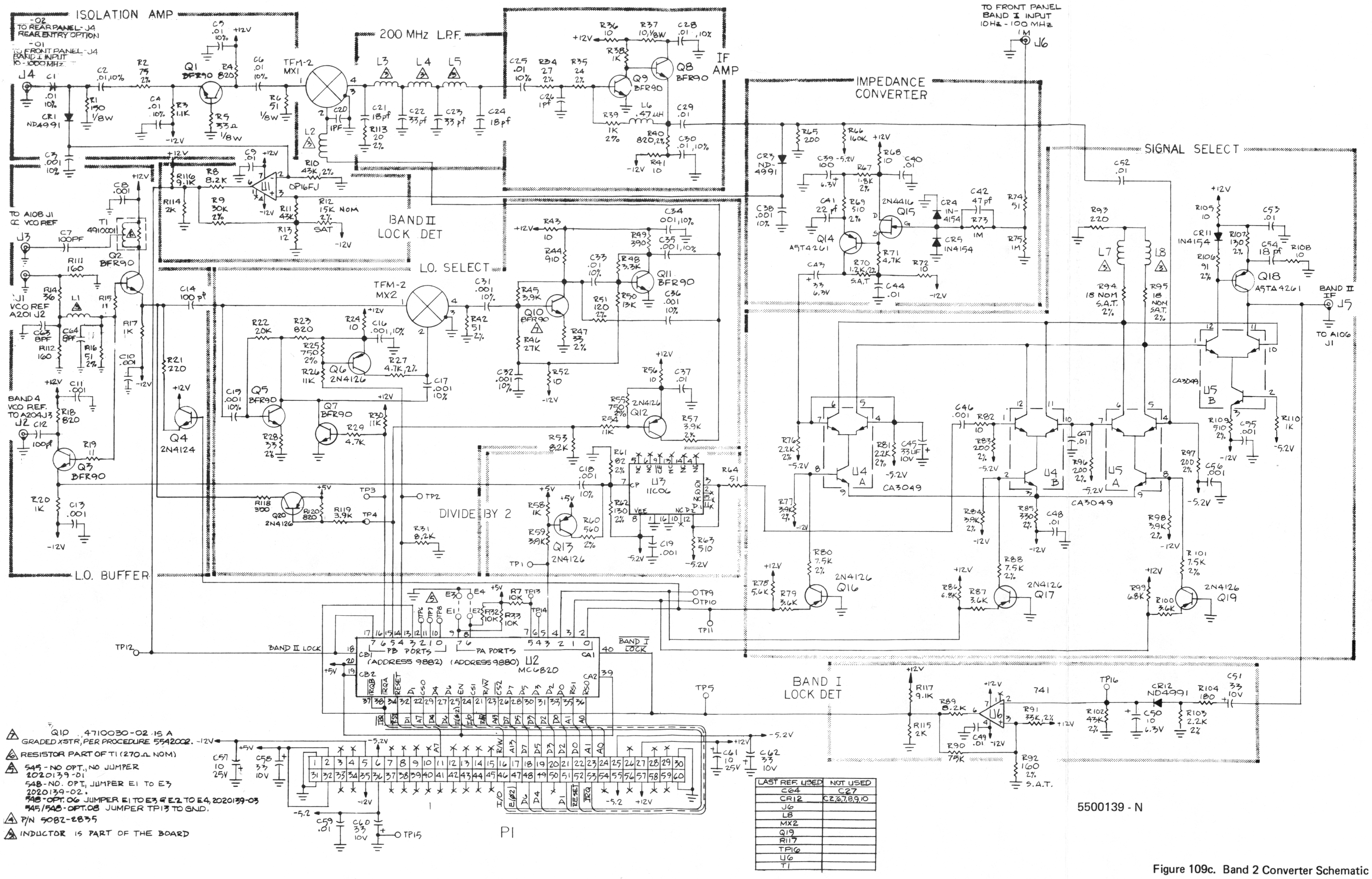
2020139 - L

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
T1	Transformer Assy	4910001	1	EIP	
TP1 thru TP16	Conn, Pin, .04D	2620032	16	460 - 2970 - 02 - 03	71279
U1	Prec, JFET Op Amplifier	3041016	1	OP16FJ	06665
U2	Periph. Interface Adaptor	3086820	1	MC6820	04713
U3	750 MHz, D-Type Flip Flop	3001106	1	11C06	07263
U4	Dual/Diff. Amplifier	3043049	2	CA3049	0000X
U5	U4				
U6	Op Amplifier	3040741	1	LM741CN	0000X


Q3
Q2
Q5
Q7
Q10
Q11
Q1
Q9
Q8
B
C
E
L6 IS TEPEE WITH R39 (REF)
TF1-16
(16)
A109
ASSY 2020139
U2
U3
U4
U5
U6
MX2
R89
C8
C14
C19
R15
E1
E2

2020139-K

Figure 109 b. Band 2 Converter Component Locator


ISOLATION AMP
TO REAR PANEL J4 REAR ENTRY OPTION
TO FRONT PANEL J4 BAND I INPUT 10-1000 MHz
J4
200 MHz L.P.F.
IF AMP
TO FRONT PANEL BAND I INPUT 10Hz - 100 MHz
J6
IMPEDANCE CONVERTER
SIGNAL SELECT
BAND II LOCK DET
TO A108 J1 CC VCO REF
J3
VCO REF A201 J2
J1
BAND 4 VCO REF. TO A204 J3
J2
L.O. SELECT
TFM-2 MX1
TFM-2 MX2
OP16FJ
U1
DIVIDE BY 2
U3 11C06
L.O. BUFFER
U2 MC6820
PB PORTS (ADDRESS 9882)
PA PORTS (ADDRESS 9880)
BAND II LOCK
BAND I LOCK
BAND I LOCK DET
741
U6
U4 A CA3049
U4 B
U5 A CA3049
U5 B
BAND II IF J5
TO A106 J1
P1
TP12
TP5
TP16
TP15
-12V
+5V
+12V
-5.2V

△7 Q10 4710030-02 IS A GRADED XSTR, PER PROCEDURE 5542002.

△6 RESISTOR PART OF T1 (270Ω NOM)

△5 545 - NO OPT., NO JUMPER 2020139-01
548 - NO. OPT., JUMPER E1 TO E3 2020139-02.
548 - OPT. 06 JUMPER E1 TO E3 & E2 TO E4, 2020139-03
545/548 - OPT. 08 JUMPER TP13 TO GND.

△4 P/N 5082-2835

△3 INDUCTOR IS PART OF THE BOARD

LAST REF. USED	NOT USED
C64	C27
CR12	C2,6,7,8,9,10
J6	
L8	
MX2	
Q19	
R117	
TP16	
U6	
T1	

5500139 - N

Figure 109c. Band 2 Converter Schematic

A110
FRONT PANEL
DISPLAY AND KEYBOARD
(2020140)

The Front Panel Display and Keyboard assembly (A110) is divided into two functional sections.

- Numeric display and annunciators
- Keyboard

NUMERIC DISPLAY AND ANNUNCIATORS

This section of the assembly contains twelve common anode 7-segment numeric display units (DS1-DS12), two green LED's (DS37 and DS38), and a maximum of twenty-four yellow LED's (DS13-DS36).

The twelve 7-segment LED's are mounted side-by-side, with space between each third digit from the right. The corresponding cathode segments of the 7-segment LED's are connected, and the drive signals come from the segment drivers Q3 through Q10. The signals to drive the digits come from the digit drivers located on the Front Panel Logic board (A111).

The twenty-four yellow LED's (DS13-DS36) are divided into three groups of 8 LED's each. The anodes of all LED's in each group are connected. The cathode of each LED in a group are connected to one of the segment drivers (Q3-Q10). With this arrangement each group of annunciator lights can be regarded as similar to one 7-segment LED. The digit drives for the 3 groups of annunciator lights also come from the Front Panel Logic board (A111).

The two green LED's (DS37 and DS38) are driven by Q1 and Q2. When these LED's light they indicate that GATE and CONVERTER SEARCH are in operation.

KEYBOARD

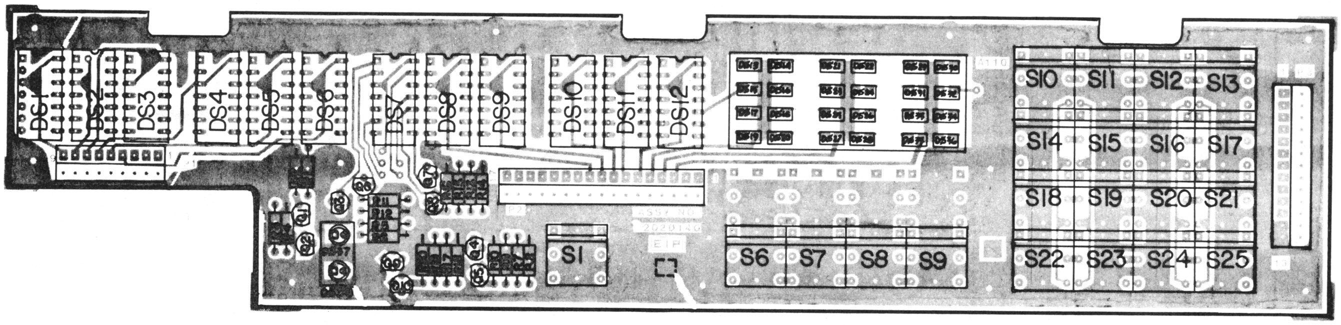
This section of the assembly contains a maximum of twenty-five (single-pole double-throw) switches. The switches are arranged in a 4 row by 6 column matrix, with the extra switch taking the row 4 column 7 position. The columns are connected to +5V through the resistor network (RN1) on the Front Panel Logic board (A111).

The keyboard is continuously scanned. The signals scanning the keyboard are derived from A111. To scan the keyboard the 4 rows are grounded sequentially. When a row is grounded, and a key in that row is pushed, one of the columns will be grounded. This information is sent to the A111 board where key debouncing is performed.

A110 FRONT PANEL DISPLAY AND KEYBOARD

2020140-B

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
Q1 thru Q10	PNP, Amp.	4710019	10	MPS - D55	04713
R1	Comp, 4.7K, 5%, 1/4 W	4010472	2	RC07GF472J	81349
R2	Comp, 130, 5%, 1/4 W	4010131	2	RC07GF131J	81349
R3	R1				
R4	R2				
R5	Comp, 240, 5%, 1/4 W	4010241	8	RC07GF241J	81349
R6	Comp, 18, 5%, 1/4 W	4010180	8	RC07GF180J	81349
R7	R5				
R8	R6				
R9	R5				
R10	R6				
R11	R5				
R12	R6				
R13	R5				
R14	R6				
R15	R5				
R16	R6				
R17	R5				
R18	R6				
R19	R5				
R20	R6				
DS1 thru DS12	LED, Numeric, Red	2800004	12	HP5082 - 7730	28480
DS13 thru DS36	LED, Lamp, Yel	2800020	24	MV57124	50522
DS37	LED, Lamp, Grn	2080018	2	MV5274	50522
DS38	DS37				
S1 S2 thru S5	Not Used				
S6 thru S25	Switch, Mon, SPDT	4500013	21	REK	
P1	9 pin Recept.	2620065	1	22 - 14 - 209	0000A
P2	17 pin Recept.	2620067	1	22 - 14 - 2171	0000A
P3	13 pin Recept.	2620066	1	22 - 14 - 212	0000A


DS1
DS2
DS3
DS4
DS5
DS6
DS7
DS8
DS9
DS10
DS11
DS12
S1
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
S17
S18
S19
S20
S21
S22
S23
S24
S25

2020140 - B

Figure 110a. Front Panel Display and Keyboard Component Locator

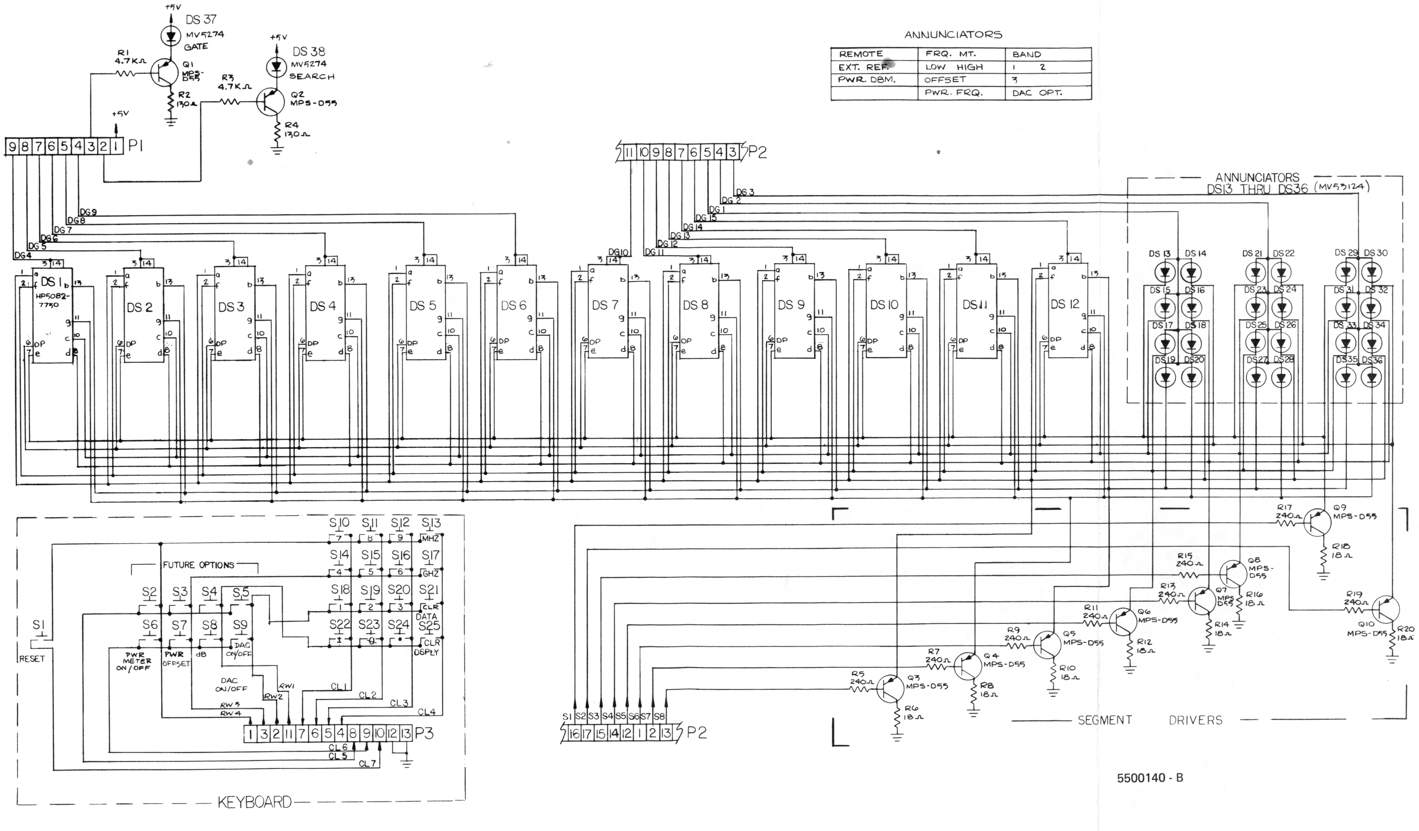

+5V
DS 37
MV5274
GATE
R1
4.7KΩ
Q1
MPS-D55
R2
130Ω
+5V
DS 38
MV5274
SEARCH
R3
4.7KΩ
Q2
MPS-D55
R4
130Ω
+5V
9 8 7 6 5 4 3 2 1 P1
ANNUNCIATORS
REMOTE
FRQ. MT.
BAND
EXT. REF.
LOW HIGH
1 2
PWR. DBM.
OFFSET
3
PWR. FRQ.
DAC OPT.
11 10 9 8 7 6 5 4 3 P2
DS3
DG2
DG1
DG15
DG14
DG13
DG12
DG11
DG10
DG9
DG8
DG7
DG6
DG5
DG4
DS 1
HP5082-7750
DS 2
DS 3
DS 4
DS 5
DS 6
DS 7
DS 8
DS 9
DS 10
DS 11
DS 12
a b c d e f g DP
ANNUNCIATORS
DS13 THRU DS36 (MV53124)
DS 13
DS 14
DS 15
DS 16
DS 17
DS 18
DS 19
DS 20
DS 21
DS 22
DS 23
DS 24
DS 25
DS 26
DS 27
DS 28
DS 29
DS 30
DS 31
DS 32
DS 33
DS 34
DS 35
DS 36
S1
RESET
FUTURE OPTIONS
S2 S3 S4 S5
S6 S7 S8 S9
PWR METER ON/OFF
PWR OFFSET
dB
DAC ON/OFF
DAC ON/OFF
S10 S11 S12 S13
7 8 9 MHZ
S14 S15 S16 S17
4 5 6 GHZ
S18 S19 S20 S21
1 2 3 CLR DATA
S22 S23 S24 S25
± 0 • CLR DSPLY
RW1
RW2
RW3
RW4
CL1
CL2
CL3
CL4
CL5
CL6
CL7
1 3 2 11 7 6 5 4 8 9 10 12 13 P3
KEYBOARD
S1 S2 S3 S4 S5 S6 S7 S8
16 17 5 14 12 1 2 13 P2
R5 240Ω
Q3 MPS-D55
R6 18Ω
R7 240Ω
Q4 MPS-D55
R8 18Ω
R9 240Ω
Q5 MPS-D55
R10 18Ω
R11 240Ω
Q6 MPS-D55
R12 18Ω
R13 240Ω
Q7 MPS D55
R14 18Ω
R15 240Ω
Q8 MPS-D55
R16 18Ω
R17 240Ω
Q9 MPS-D55
R18 18Ω
R19 240Ω
Q10 MPS-D55
R20 18Ω
SEGMENT DRIVERS
5500140 - B

Figure 110b. Front Panel Display and Keyboard Schematic

A111
FRONT PANEL LOGIC
(2020191)

The Front Panel Logic assembly (A111) contains logic circuitry for control of two functions.

- DISPLAY CONTROL
- KEYBOARD CONTROL

The +5 V power supply to the front panel assemblies (A110 and A111) is regulated by a voltage regulator that is located behind the A111 board. For heatsinking purposes, this voltage regualtor is mounted on the chassis. Please refer to figure 111b. Front Panel Logic block diagram on page 111-3.

DISPLAY CONTROL

The twelve 7-segment LEDs and the three groups of annunciator lights on A110 are multiplexed. To turn on a particular segment in a digit, both the digit driver for that digit and the segment driver for that segment must be on.

The display logic is in constant operation in either the self-scan mode or the memory update mode.

SELF-SCAN MODE

This is the normal operating mode. In this mode the display scan clock is clocking the display counter (U6). The state of the display counter determines which digit will be turned on.

The state of the display counter is decoded by 4 to 16 line multiplexer (U2), and the appropriate digit driver is turned on. At this time the display memory (U7 and U8) is read, and the on/off information (stored in the display memory for that specific digit), turns the segment drivers (A110) on or off.

The display intensity is controlled by varying the duty cycle of the multiplexing. This is done by varying the resistance of the potentiometer (R4) which, in turn, varies the length of time the decoder (U2) and the display memories (U7, U8) are disabled between each scan clock cycle.

At the start of each gate operation the GATE light control is triggered, and the GATE LED lights for the length of the GATE.

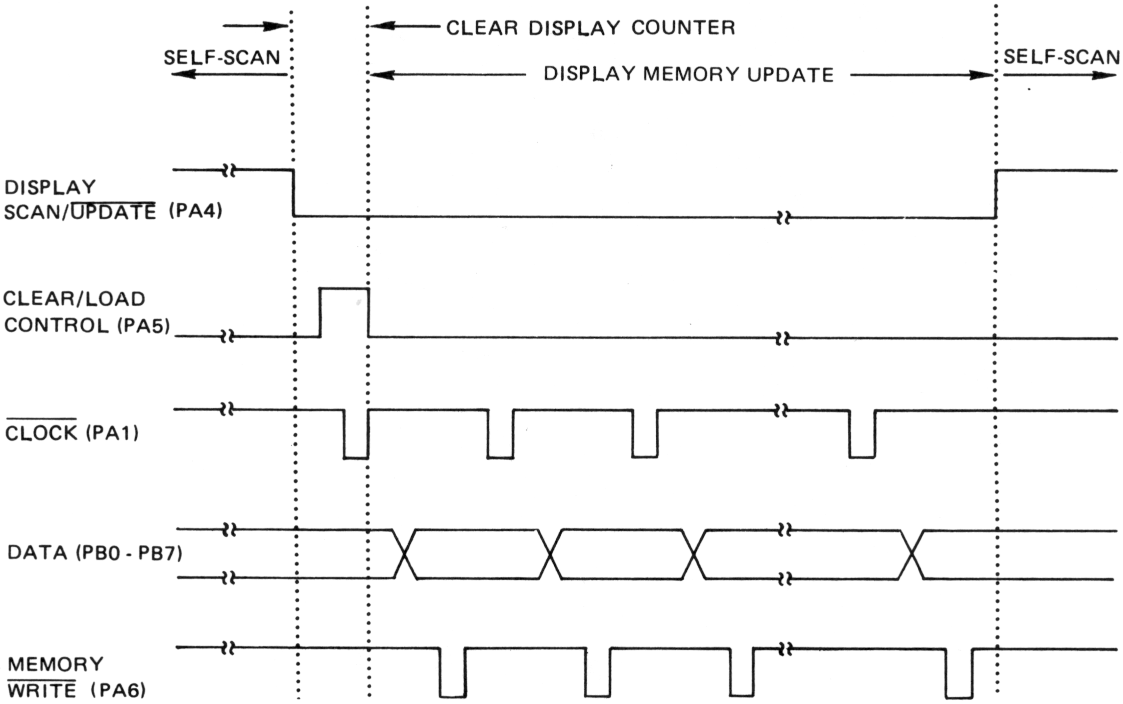
MEMORY UPDATE MODE

In this mode the multiplexer logic is disabled by setting the display scan/$\overline{\text{update}}$ control line (PA4) to logic 0. The microprocessor controlled clock ($\overline{\text{clock,}}$ PA1) is used to clock the display counter(U6).

Before updating the display memory (U7 and U8), the display counter is cleared by setting the clear/load control line (PA5) to logic 1, and clocking the clock input of U6. Update mode timing is illustrated in figure 111a.

KEYBOARD CONTROL

When the keyboard is not being read by the microprocessor, the Keyboard READ/$\overline{\text{SCAN}}$ control line (PA0) is at logic 0. All the outputs of the shift register are at logic 0. If no key on the keyboard is pushed, all the inputs to the 8-input NAND gate (U13) are at logic 1 level. When a key is pushed, the column containing that key will be grounded. The output of U13 goes to logic 1 and C7 (in the debounce circuit) starts to discharge. When the voltage accross C7 reaches approximately +0.7 V above ground, the debounce circuit will trigger the interrupt input on the PIA (U11, pin 18) indicating that a key is being pushed.



SELF-SCAN
CLEAR DISPLAY COUNTER
DISPLAY MEMORY UPDATE
SELF-SCAN
DISPLAY SCAN/UPDATE (PA4)
CLEAR/LOAD CONTROL (PA5)
CLOCK (PA1)
DATA (PB0 - PB7)
MEMORY WRITE (PA6)

Figure 111a. Memory Update Mode Sequence

READ KEYBOARD

When the microprocessor needs to read the keyboard, a logic 1 is put on the keyboard READ/$\overline{\text{SCAN}}$ control line (PA0). This enables the data buffer (U9). A 0111 is then loaded into the shift register (U3) by putting a logic 1 on the CLEAR/LOAD control line (PA5) and clocking the clock input of U3. The logic 0 at the output of the shift register (U3) is shifted through the shift register once. The microprocessor reads the keyboard row and column information with the logic 0 at each of the 4 outputs of U3 to determine the coordinate of the key pushed. After the keyboard is read, the keyboard READ/$\overline{\text{SCAN}}$ line is returned to logic 0.

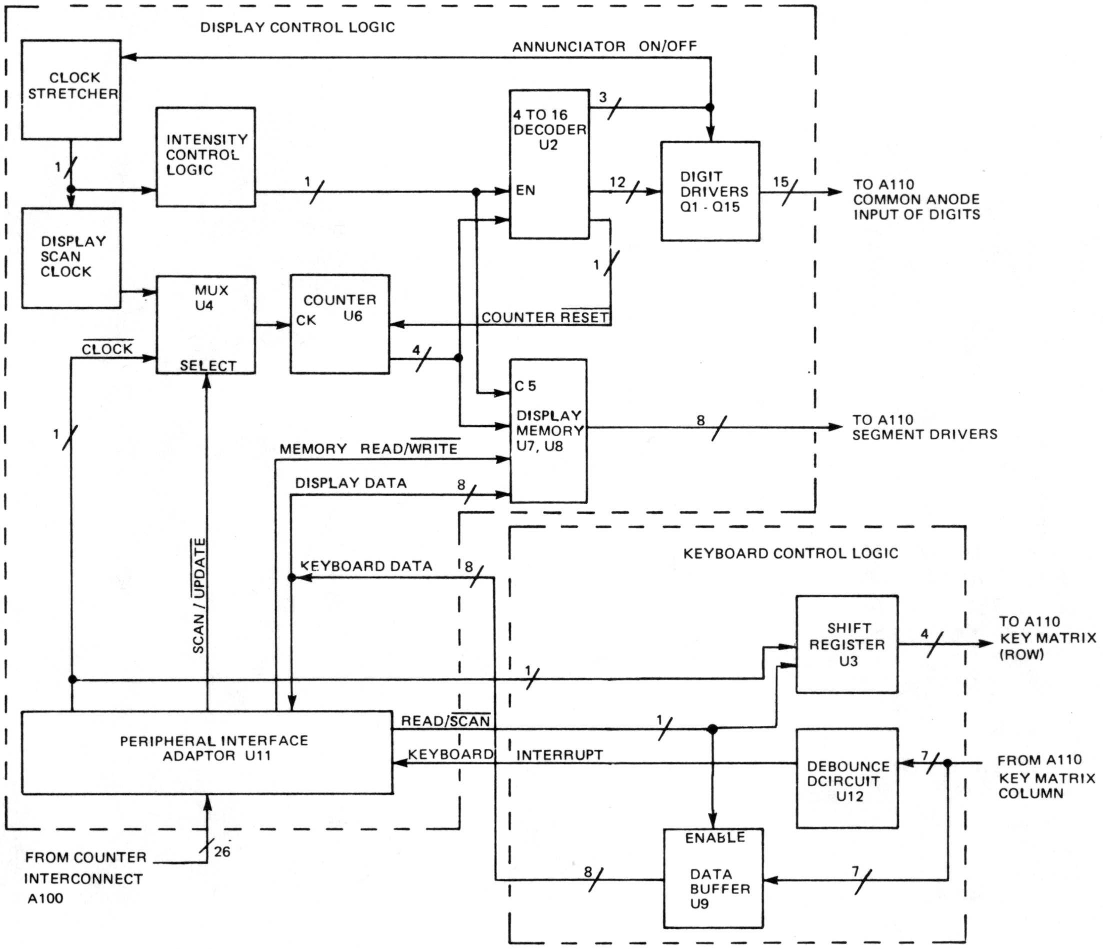

DISPLAY CONTROL LOGIC
ANNUNCIATOR ON/OFF
CLOCK STRETCHER
INTENSITY CONTROL LOGIC
4 TO 16 DECODER U2
EN
3
12
1
DIGIT DRIVERS Q1 - Q15
15
TO A110 COMMON ANODE INPUT OF DIGITS
DISPLAY SCAN CLOCK
MUX U4
SELECT
COUNTER CK U6
COUNTER RESET
4
$\overline{\text{CLOCK}}$
C5
DISPLAY MEMORY U7, U8
8
TO A110 SEGMENT DRIVERS
MEMORY READ/$\overline{\text{WRITE}}$
DISPLAY DATA
KEYBOARD DATA
SCAN/$\overline{\text{UPDATE}}$
KEYBOARD CONTROL LOGIC
SHIFT REGISTER U3
TO A110 KEY MATRIX (ROW)
PERIPHERAL INTERFACE ADAPTOR U11
READ/$\overline{\text{SCAN}}$
KEYBOARD
INTERRUPT
DEBOUNCE DCIRCUIT U12
7
FROM A110 KEY MATRIX COLUMN
ENABLE
DATA BUFFER U9
26
FROM COUNTER INTERCONNECT A100

Figure 111b. Front Panel Logic Block Diagram

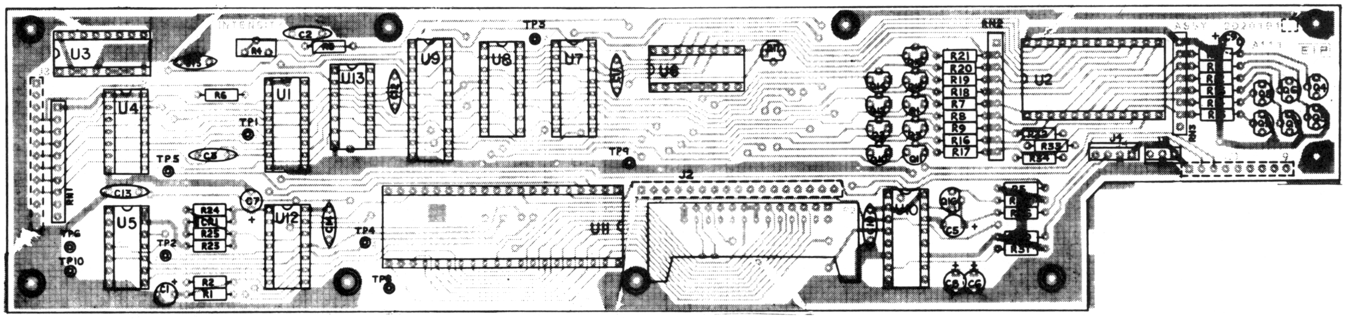
A111 FRONT PANEL DRIVER

2020191 - A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A111	Front Panel Driver Assy	2020191	1	EIP	
C1	Tant, 0.1μF, 10%, 35V	2300020	1	TAPA .10M35	14433
C2	Cer., .002μF, 20%, 1KV	2150005	2	TG - S20	56289
C3	C2				
C4	Not Used				
C5	Tant, 47μF, 20%, 16V	2300025	1	TAPA 47M16	14433
C6	Tant, 2.2μF, 20%, 16V	2300012	1	TAPA 2.2M16	14433
C7	Tant, 22μF, 20%, 16V	2300030	1	TAPA 22M16	14433
C8	Tant, .33μF, 20%, 35V	2310031	1	TAPA .33M16	14433
C9	Tant, 33μF, 20%, 10V	2300015	1	TAPA 33M16	14433
C10 thru C15	Cer., .01μF, 20%, 100V	2150003	6	TG - S10	56289
CR1	General Purpose	2704154	1	IN4154	07263
J1	9 Pin Male	2620062	1	22 - 03 - 2091	0000B
J2	17 Pin Male	2620064	1	22 - 03 - 2171	0000B
J3	13 Pin Male	2620063	1	22 - 03 - 2131	0000B
J4	4 Pin, FR. LOCK	2620068	1	640456-4	74868
J5	3 Pin	2620121	1	640456-3	74868
P2	26 Pin, Right Angle	2620131	1	3493 - 1002	76381
Q1 thru Q15	PNP, Power	4710027	15	MPS - D54	04713
Q16	NPN, General Purpose	4704124	2	2N4124	04713
Q17	Q16				
R1	Comp, 10K, 5%, 1/4W	4010103	2	RC07GF103J	81349
R2	Comp, 220, 5%, 1/4W	4010221	1	RC07GF221J	81349
R3	Comp, 75K, 5%, 1/4W	4010753	1	RC07GF753J	81349
R4	Variable, Cer., 200K	4250022	1	72XR200	73138
R5	Comp, 120K, 5%, 1/4W	4010124	1	RC07GF124J	81349
R6	Comp, 2.4K, 5%, 1/4W	4010242	1	RC07GF242J	81349
R7 thru R21	Comp, 1K, 5%, 1/4W	4010102	15	RC07GF102J	81349
R22	Not Used				
R23	Comp, 15K, 5%, 1/4W	4010153	1	RC07GF153J	81349
R24	Comp, 390, 5%, 1/4W	4010391	1	RC07GF391J	81349
R25	Comp, 200, 5%, 1/4W	4010201	1	RC07GF201J	81349
R26	Comp, 820, 5%, 1/4W	4010821	1	RC07GF821J	81349
R27	R1				
R28	Not Used				
R29	Comp, 2.2K, 5%, 1/4W	4010222	1	RC07GF222J	81349
R30	Not Used				
R31	Comp, 27K, 5%, 1/4W	4010273	1	RC07GF273J	81349
R32 thru R34	Comp, 39K, 5%, 1/4W	4010393	3	RC07GF393J	81349
RN1	Network, 10K	4170003	2	785-1-R10K	32997
RN2	RN1				
RN3	Network, 10K	4170004	1	784-1-R10K	32997

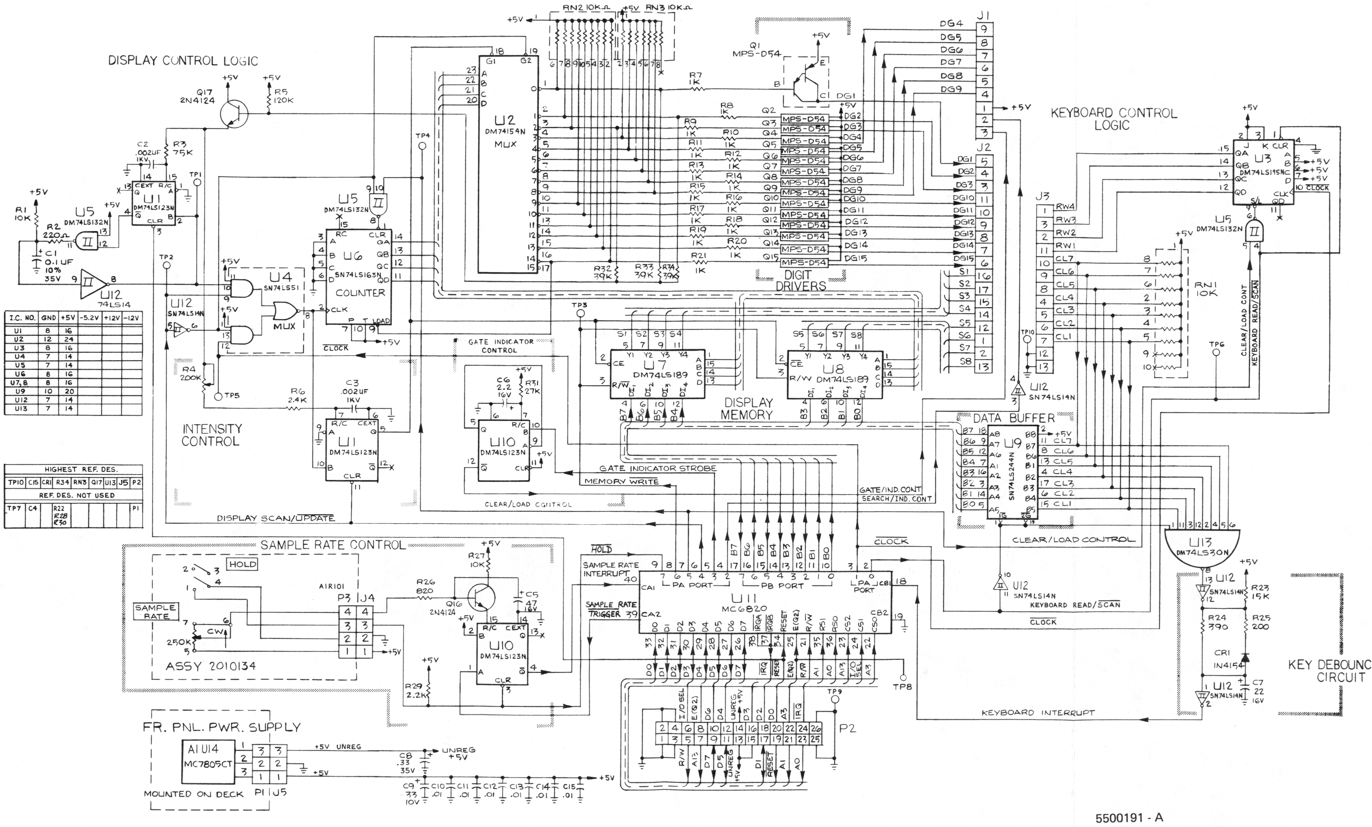
A111 FRONT PANEL DRIVER continued

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
TP1 thru TP6	.040D Pin	2620032	9	460-2970-02-03	71279
TP7	Not Used				
TP8 thru TP10	TP1				
U1	TTL, Monostable, MV	3084123	2	DM74LS123N	0000X
U2	4-16 Line Decoder	3074154	1	DM74154N	0000X
U3	4 Bit Shift Register	3084195	1	DM74LS195N	0000X
U4	AND - OR - INVERT Gates	3087451	1	SN74LS51N	01295
U5	Quad, 2 INP NAND Gate	3084132	1	DM74LS132N	0000X
U6	Binary Sync Clear	3084163	1	SN74LS163	01295
U7	Bipolar RAMS	3057489	2	DM74LS189	0000X
U8	U7				
U9	Oct Bus Trans	3084244	1	SN74LS244N	01295
U10	U1				
U11	Periph, Interface Adaptor	3086820	1	MC6820	04713
U12	Hex Inverter	3087414	1	SN74LS14N	01295
U13	8INP NAND Gates	3087430	1	DM74LS30N	0000X
U14	Pos. Voltage Regulator (reference only - U14 part of front panel power supply)	3057805	1	MC7805CT	04713


U3
U4
U5
U1
U13
U9
U8
U7
U6
U2
U12
U11
U10
J2
TP1
TP2
TP3
TP4
TP5
TP6
TP8
TP9
TP10
R1
R2
R4
R5
R6
C2
C3
C13
C1
C5
C6
C8
R24
R25
R7
R8
R9
R16
R17
R18
R19
R20
R21
R33
R34
R31
RN1
RN2
RN3
J1

2020191 - A

Figure 111c. Front Panel Component Locator


DISPLAY CONTROL LOGIC
INTENSITY CONTROL
SAMPLE RATE CONTROL
KEYBOARD CONTROL LOGIC
DIGIT DRIVERS
DISPLAY MEMORY
DATA BUFFER
KEY DEBOUNCE CIRCUIT
FR. PNL. PWR. SUPPLY
MOUNTED ON DECK
ASSY 2010134
U2 DM74154N MUX
U6 SN74LS163N COUNTER
U4 SN74LS51 MUX
U1 DM74LS123N
U5 DM74LS132N
U12 74LS14
U7 DM74LS189
U8 DM74LS189
U9 SN74LS244N
U10 DM74LS123N
U11 MC6820
U3 DM74LS195N
U13 DM74LS30N
A1U14 MC7805CT
Q1 MPS-D54
Q17 2N4124
Q16 2N4124
RN1 10K
RN2 10K
RN3 10K
J1
J2
J3
J4
J5
P1
P2
P3
HOLD
SAMPLE RATE
GATE INDICATOR CONTROL
GATE INDICATOR STROBE
MEMORY WRITE
CLEAR/LOAD CONTROL
DISPLAY SCAN/UPDATE
GATE/IND.CONT
SEARCH/IND.CONT
CLOCK
KEYBOARD READ/SCAN
KEYBOARD INTERRUPT
SAMPLE RATE INTERRUPT
SAMPLE RATE TRIGGER
PA PORT
PB PORT
+5V UNREG
5500191 - A

I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U1	8	16			
U2	12	24			
U3	8	16			
U4	7	14			
U5	7	14			
U6	8	16			
U7, 8	8	16			
U9	10	20			
U12	7	14			
U13	7	14			

HIGHEST REF. DES.								
TP10	C15	CR1	R34	RN3	Q17	U13	J5	P2
REF. DES. NOT USED								
TP7	C4		R22 R28 R30					P1

Figure 111d. Front Panel Logic Schematic

A203
BAND 3 MICROWAVE CONVERTER

The A203 Microwave Converter consists of three sub-assemblies.

- A201A Voltage Control Oscillator
- A201B IF Amplifier
- A202 Microwave (yig)

CAUTION

Disassembly of the A202 Microwave assembly, or removal of it from the A201A VCO or A201B IF Amplifier will void the EIP warranty.

The assembly drawing and schematic for both the VCO and IF circuits are included only for reference. The entire A203 assembly must be tested as a complete unit to ensure proper performance of the counter. Repair of the A202 Microwave assembly can only be done at the factory. The VCO and IF Amplifier boards require special test equipment, therefore field repair is not recommended.

The Band 3 Converter is a complete microwave subsystem (see Figure 203-1) which converts an input signal in the 1 to 18 (26.5) GHz range down to an IF of 125MHz. Down conversion is achieved in this heterodyne system by combining the input signal with a harmonic of a precisely known reference signal (F_{VCO}). The mixer then produces a signal (F_{IF}) equal to the difference between the input and reference harmonic. If this difference is close to 125MHz, it is amplified to a level of about 0dBm and then counted. The input signal is then determined from the equation $F_{IN} = NF_{VCO} + F_{IF}$. F_{VCO} is set by the instrument program via a phase locked loop located on the converter control board (A108) and is thus known exactly. Harmonics of the VCO are produced by the comb generator and coupled to the mixer. The frequency ranges of the VCO and IF are such that for any VCO frequency and any input frequency, only one harmonic can produce an IF frequency. The YIG filter located between the RF input and the mixer is used to approximatley determine the input frequency and from this information the desired values of N, F_{VCO} and +/— are determined.

Two other outputs are obtained from the Band 3 Converter. The first is an anlaog signal which is a measure of input RF power. The second is a digital signal $\overline{\text{(IF THRESHOLD)}}$ which indicates that an IF signal exists at a level of —3dBm or greater.

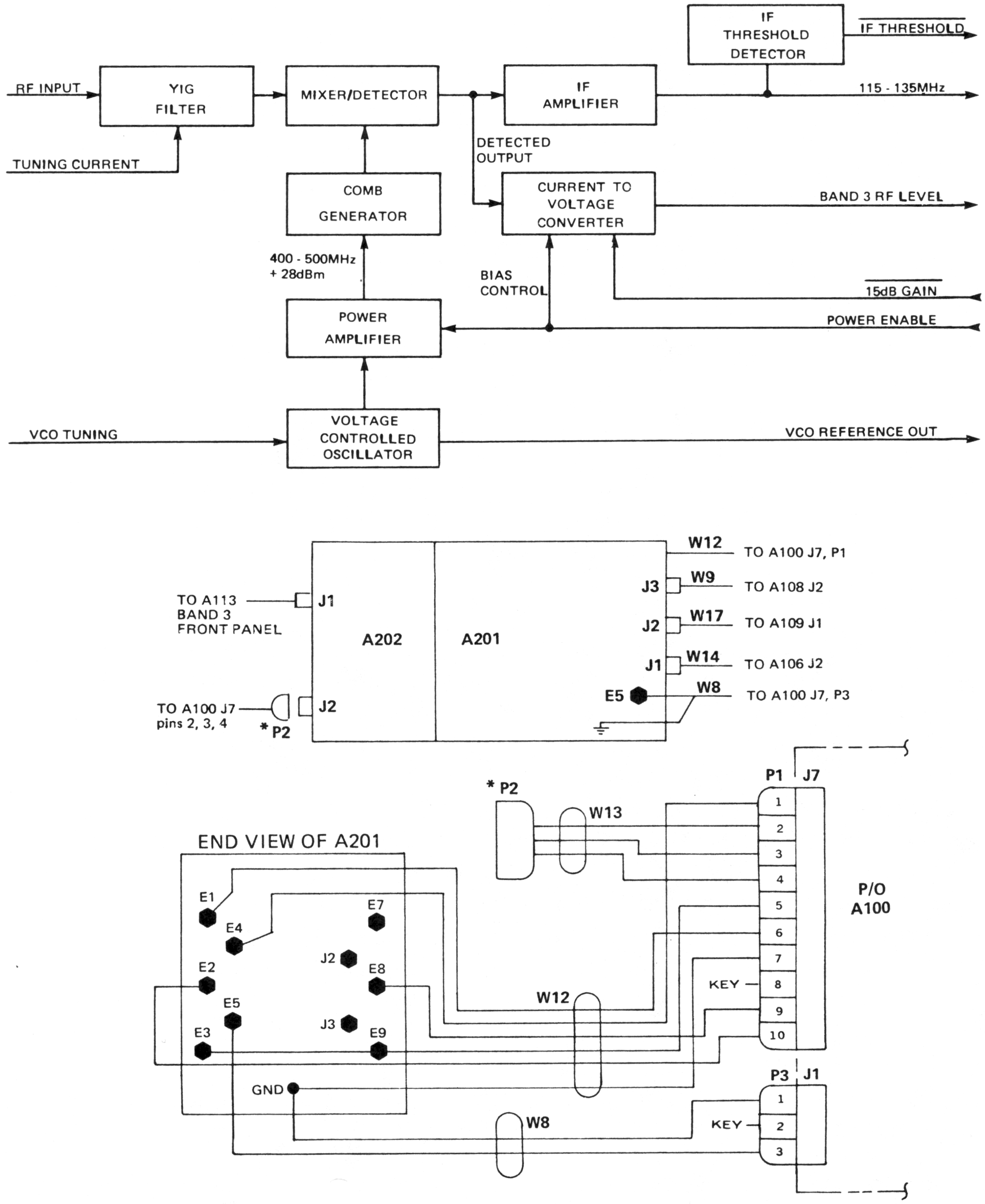

RF INPUT
YIG FILTER
TUNING CURRENT
MIXER/DETECTOR
COMB GENERATOR
400 - 500MHz
+ 28dBm
POWER AMPLIFIER
VOLTAGE CONTROLLED OSCILLATOR
VCO TUNING
VCO REFERENCE OUT
IF AMPLIFIER
IF THRESHOLD DETECTOR
IF THRESHOLD
115 - 135MHz
DETECTED OUTPUT
CURRENT TO VOLTAGE CONVERTER
BAND 3 RF LEVEL
BIAS CONTROL
15dB GAIN
POWER ENABLE
A202
A201
TO A113 BAND 3 FRONT PANEL
J1
TO A100 J7 pins 2, 3, 4
J2
* P2
W12
TO A100 J7, P1
J3
W9
TO A108 J2
J2
W17
TO A109 J1
J1
W14
TO A106 J2
E5
W8
TO A100 J7, P3
END VIEW OF A201
E1
E4
E7
E2
J2
E8
E5
E3
J3
E9
GND
* P2
W13
W12
W8
P1
J7
1
2
3
4
5
6
7
KEY
8
9
10
P/O A100
P3
J1
1
KEY
2
3

Figure 203-1. Band 3 Microwave Converter Diagram

A201A
VOLTAGE CONTROL OSCILLATOR
(2020142)

The VCO Assembly contains three sub-functions as shown in Fig. 201A-1. The VCO consists of a transistor oscillator (Q1), whose frequency is determined by an inductor (L1) and a variable capacitor (CR2). The capacitance of CR2 is determined by the applied tuning voltage at J3. For increased stability and noise reduction, an internal voltage regulator (R3, C4, CR3) is used.

The second function is performed by a single stage common base amplifier that is broadly tuned and loaded with 50 ohms. The output level is approximately + 8 dBm over the range 370 - 500MHz. This output is the VCO reference.

The third function is performed by a three stage power amplifier consisting of a common base amplifier (Q3) and two class C stages, Q4 and Q5. This amplifier provides approximately 20dB of gain and 0.6 watts output over the tuning range 400 to 500MHz. The variable capacitors C17, C25, and C28 are adjusted to optimize output power and flatness. Output power is switched on or off by the Pin switch CR3, CR4 which is controlled by U1. On to off power ratio is in excess of 50dB.

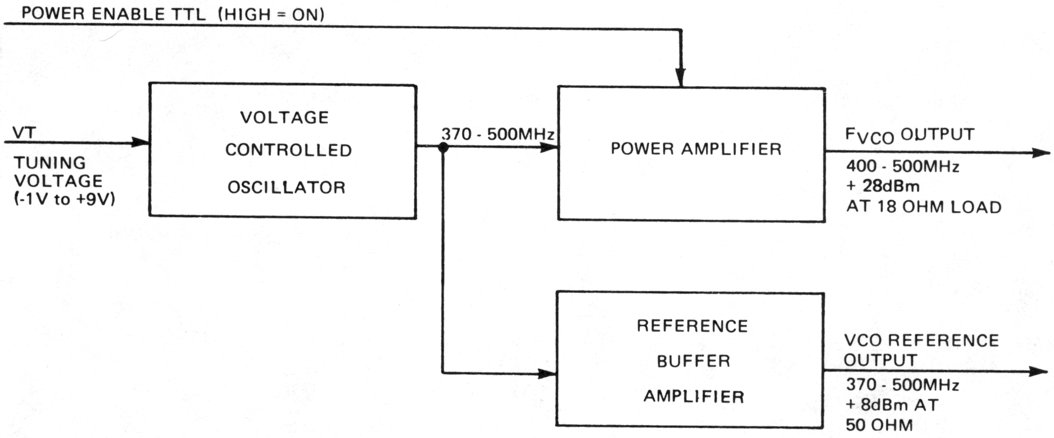

POWER ENABLE TTL (HIGH = ON)
VT
TUNING VOLTAGE (-1V to +9V)
VOLTAGE CONTROLLED OSCILLATOR
370 - 500MHz
POWER AMPLIFIER
F_{VCO} OUTPUT
400 - 500MHz
+ 28dBm
AT 18 OHM LOAD
REFERENCE BUFFER AMPLIFIER
VCO REFERENCE OUTPUT
370 - 500MHz
+ 8dBm AT
50 OHM

Figure 201A-1. VCO Block Diagram

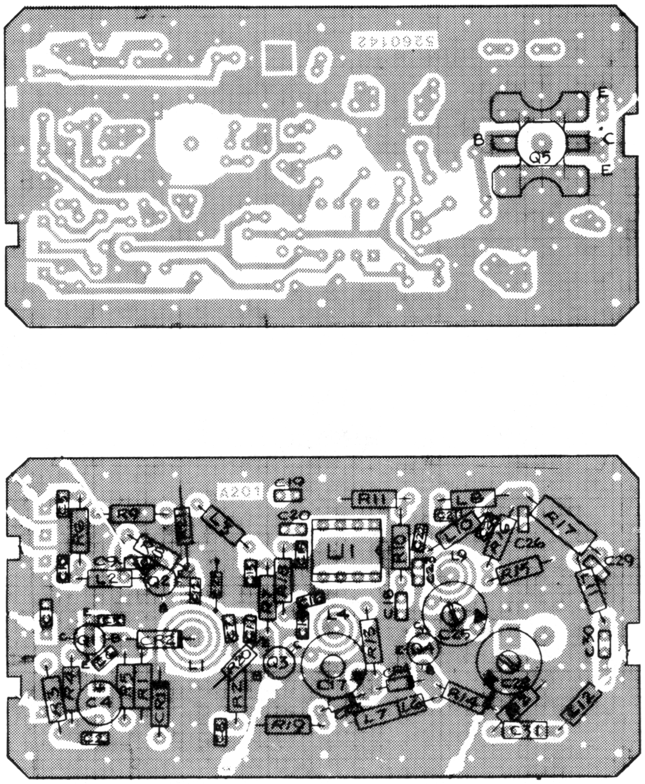
A201A VOLTAGE CONTROL OSCILLATOR

2020142-P

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A201A	Voltage Control Oscillator Assy	2020142	1		
	P/O VCO/IF Module Assy 203	2010142	Ref		
C1	Cer, .001μF, 10%, 100V	2150015	16	6183X7R102KA100	80031
C2	C1				
C3	Cer, 4.7pF, 25%, 100V	2150086	1	6113COG689DA100	80031
C4	Tant, 33μF, 20%, 20V	23000023	1	TAG20 - 30/20%	14433
C5	C1				
C6	Cer, 6.8pF, 25%, 100V	2150087	1	6113COG689DA100	80031
C7					
thru					
C10	C1				
C11	Cer, 100pF, 10%, 180V	2150056	1	6183X7R101KA100	80031
C12	Cer, 33pF, 10%, 100V	2150069	1	6183COG330KA100	80031
C13	C1				
C14	Cer, .01μF, 10%, 100V	2150014	4	6123X7R103KA100	80031
C15	C1				
C16	C14				
C17	Var, 2-8pF, 250V	2350001	1	10S-T-22-2/8	0000B
C18					
thru					
C21	C1				
C22	C14				
C23	C14				
C24	C1				
C25	Var, 5.5, 18pF, 250V	2350002	2	10S-T-22-02	0000B
C26	C1				
C27	Cer, 22pF	2150067	1	6183COG220KA100	80031
C28	C25				
C29	C1				
C30	X7R, 47pF	2150039	1	6113X7R470KA100	80031
C31	Nom. S.A.T. , 5pF	2260999	1	DM10	56289
C32	Mica, S.A.T. Nom 1pF	2269999	1		
CR1	Zener, 9.1V	2730960	1	1N960B	04713
CR2	Tun, UHF/VHF HYPERABRPT	2710037	1	ZC800	18518
CR3	Pin	2710024	2	MA47123	
CR4	CR3				
L1	Part of Board				
L2	.39μH	3150014	1	1025-10	72259
L3	1.0μH	3150003	4	DD-1.00	72259
L4	L1				
L5	Nom. 056, S.A.T.	3529999	1		
L6	Ferrite Bead	3500011	1	56-590-65/33	
L7	0.1μH	3510001	2	DD-0.10	72259
L8	L3				
L9	L1				
L10	L3				
L11	L3				
L12	L7				
Q1	Microwave Transistor	4710032	3	NE02137	0000S
Q2	Q1				
Q3	Q1				
Q4	NPN, RF	4710030	1	BFR-90-MOT	04713
Q5	UHF/VHF NPN Power	4710029	1	NE050391-12	0000S

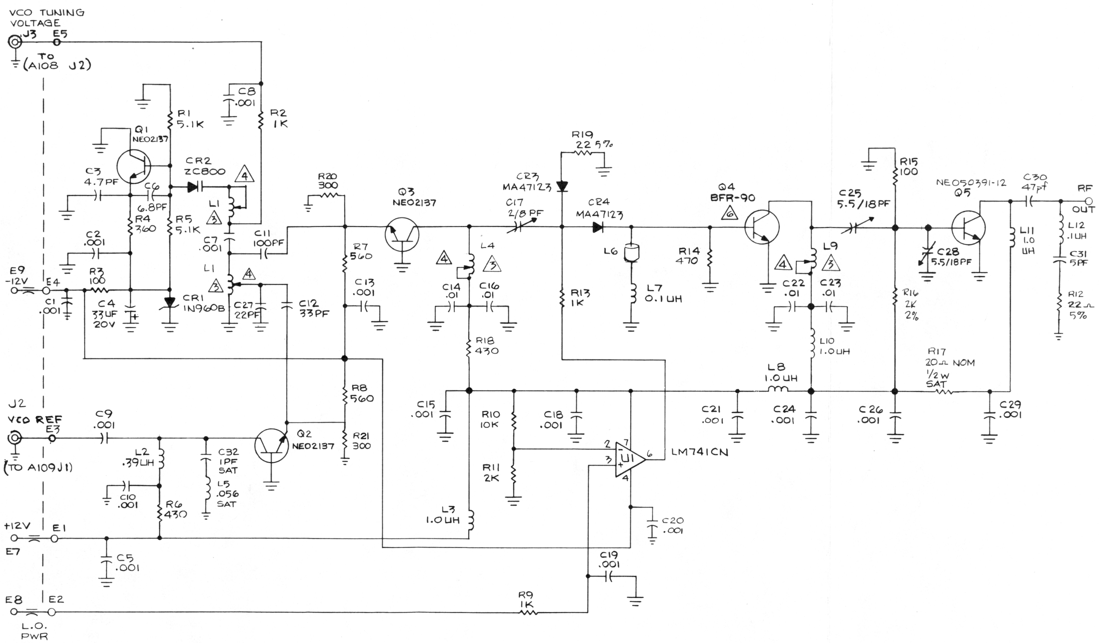
A201A VOLTAGE CONTROL OSCILLATOR, continued

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R1	Met Ox, 5.1K, 2%, 1/4 W	4130512	2	C4/2%/5.1K	24546
R2	Met Ox, 1K, 2%, 1/4 W	4130102	3	C4/2%/1K	24546
R3	Met Ox, 100, 2%, 1/4 W	4130101	2	C4/2%/100	24546
R4	Met Ox, 360, 2%, 1/4 W	4130361	1	C4/2%/360	24546
R5	R1				
R6	Met Ox, 430, 2%, 1/4 W	4130431	2	C4/2%/430	24546
R7	Met Ox, 560, 2%, 1/4 W	4130561	2	C4/2%/560	24546
R8	R7				
R9	R2				
R10	R2				
R11	Met Ox, 2K, 2%, 1/4 W	4130202	2	C4/2%/2K	24546
R12	Comp, 22 ohm, 5%, 1/8W	4000220	1	RC05GF220J	81349
R13	R2				
R14	Met Ox, 470, 2%, 1/4 W	4130471	1	C4/2%/470	24546
R15	R3				
R16	R11				
R17	Comp, 20 ohm, 5%, 1/2 W (SAT)	4020999	1	RC07GFXXX	81349
R18	R6				
R19	Carbon, 22, 5%,	4010220	1		
R20	Met Ox, 300 ohm, 2%	4130301	2	C4/2%/300	
R21					
U1	Lin Op Amplifier	3040741	1	LM741CN	0000X


5260142
E
B
Q5
C
E
A201
C19
R11
L8
R9
L5
C20
U1
R10
C21
L10
R17
C26
C29
L2
Q2
L9
R15
L4
C18
C25
CR2
L1
Q3
R13
C4
C17
C30
R14
L7
L6
R19
C31
L12
C2

2020142 - P

Figure 201A-2. Voltage Controlled Oscillator Component Locator


VCO TUNING
VOLTAGE
J3
E5
TO
(A108 J2)
C8
.001
R2
1K
R1
5.1K
Q1
NE02137
CR2
ZC800
△4
C3
4.7PF
C6
6.8PF
L1
△3
R4
360
R5
5.1K
C7
.001
C11
100PF
C2
.001
L1
△3
△4
E9
-12V
E4
R3
100
C1
.001
C4
33UF
20V
CR1
1N960B
C27
22PF
C12
33PF
R20
300
Q3
NE02137
R7
560
C13
.001
R8
560
R21
300
J2
VCO REF
E3
C9
.001
(TO A109J1)
L2
.39UH
C32
1PF
SAT
L5
.056
SAT
C10
.001
R6
430
Q2
NE02137
+12V
E1
E7
C5
.001
E8
E2
L.O.
PWR
CONTROL (TO A108 VIA 100J7)
R19
22 5%
CR3
MA47123
C17
2/8 PF
CR4
MA47123
L4
△4
△3
C14
.01
C16
.01
R18
430
C15
.001
R10
10K
C18
.001
R11
2K
L3
1.0UH
R13
1K
L6
L7
0.1UH
R14
470
2
7
3
U1
6
4
LM741CN
C20
.001
C19
.001
R9
1K
Q4
BFR-90
△6
L9
△4
△3
C22
.01
C23
.01
L10
1.0UH
L8
1.0UH
C21
.001
C24
.001
C25
5.5/18PF
R15
100
R16
2K
2%
C26
.001
C28
5.5/18PF
NE050391-12
Q5
C30
47pf
RF
OUT
L11
1.0
UH
L12
.1UH
C31
5PF
R12
22Ω
5%
R17
20Ω NOM
1/2W
SAT
C29
.001

△6 Q4 4710030-02 IS A GRADED XSTR PER PROCEDURE 5542002.

△5 R17, 20Ω NOMINAL, SAT RANGE 1Ω TO 24Ω. REFER TO TEST PROCEDURE FOR SELECTION CRITERIA (5540142).

△4 SELECT AT TEST ADJUSTMENT

△3 PART OF P.C. BOARD.

5500142 - N

Figure 201A-3. Voltage Controlled Oscillator Schematic

A201B
IF AMPLIFIER
(2020143)

The IF Amplifier performs three major functions.

- Amplifies the down-converted intermediate IF frequency to ± 0dBm.
- Provides a digital threshold output when the IF power exceeds -3dBm.
- Provides an analog signal that is proportional to the total power at the Band 3 input. A gain scaling control alters the output by 15dB (=X30).

The Microwave assembly mixer output is the input to the IF board. The IF goes through a high pass filter to three similar amplifier stages. Stage 1 consists of transistors Q1 and Q2 operating under closed loop feedback via R4. Resonant peaking of the output at 125MHz using L4 and C8 gives a power gain of 23dB. Successive stages are similar except that stagger tuning is used for optimum response shape. Inductors L4, L5, and L7 are printed on the circuit board and are adjusted by means of shorting bars placed across portions of the spiral. The IF output signal is sampled by a detector CR3. It's level is compared to a voltage corresponding to –3dBm. When this level is exceeded, the IF threshold output goes low.

The low frequency signal from the mixer is the current caused by rectification of the input power. This is converted to a voltage in U2. To provide a larger dynamic range, a gain change is made by switching the Field Effect Transistor (FET) Q7, thus lowering the feedback resistor. Assemblies used in –02 converters (26.5 GHz) also include transistors Q8 & Q9 to translate a TTL input to ± 12V necessary to drive FET Q10. This circuit sets the mixer bias current to 0 when the VCO power amplifier is enabled.

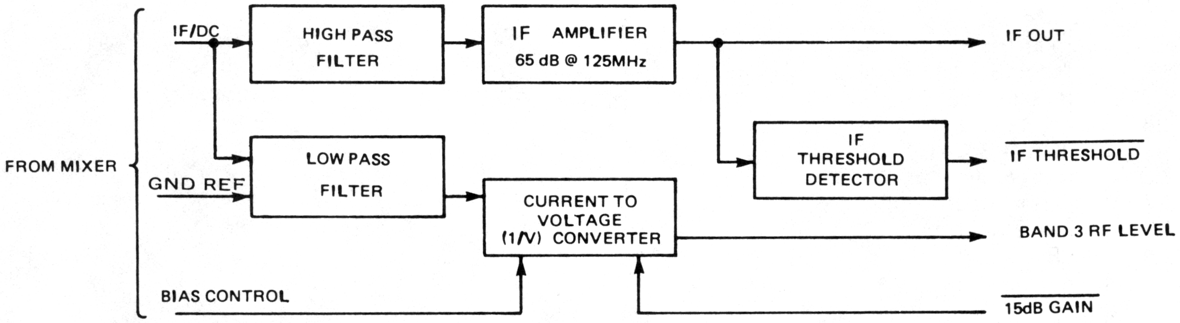

FROM MIXER
IF/DC
GND REF
BIAS CONTROL
HIGH PASS FILTER
IF AMPLIFIER 65 dB @ 125MHz
LOW PASS FILTER
CURRENT TO VOLTAGE (I/V) CONVERTER
IF THRESHOLD DETECTOR
IF OUT
IF THRESHOLD
BAND 3 RF LEVEL
15dB GAIN

Figure 201B-1. IF Amplifier Functional Diagram

A201B IF AMPLIFIER

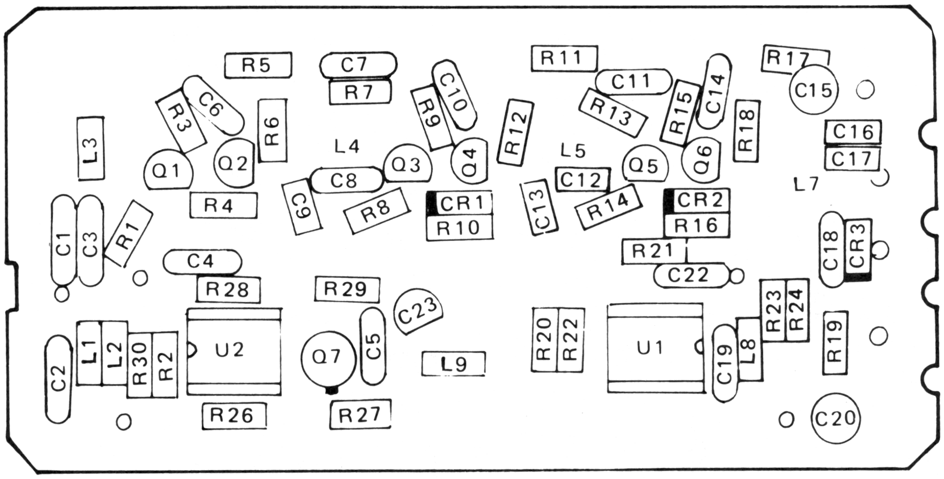
2020143- T

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A201B	IF Amplifier Assy	2020143	1		
	P/O VCO/IF Mod Assy	2010142	Ref		
C1	Mica, 8pF, 5%, 500V	2260011	1	CD080C03	56289
C2	Mica, 100pF, 5%, 500V	2260034	6	FD101J03	72136
C3	Mica, 12pF, 5%, 500V	2260013	2	CD120J03	56289
C4	Cer, .01μF, 20%	2150003	7	TG - S10	56289
C5	Not Used				
C6	Cer, .01μF, 20%, 100V	2150003	6	TG - S10	56289
C7	C4				
C8	Mica, 33pF, NOM S.A.T.	2269999	1	CD10	56289
C9	C2				
C10	C4				
C11	C4				
C12	Mica, S.A.T., 47pF, 5%, NOM	2269999	1	DM - 10	72136
C13	C2				
C14	C4				
C15	Tant, 10μF, 20%, 25V	2300029	2	TAG20 - 10/25(M)	14433
C16	Mica, 39pF, 5%,	2260023	1	CD10ED390J03	56289
C17	C2				
C18	C2				
C19	C4				
C20	C15				
C21	Not Used				
C22	C2				
C23	Cer, .001μF, 10%, 100V	2150015	1	UR20205100X7R102K	80031
CR1	Hot Carrier	2710004	2	FH1100	07263
CR2	CR1				
CR3	Zero Bias Shottky	2710038	1	ND4991	21843
L1	Inductor, 0.1μH	3510001	1	DD - 0.10	72259
L2	Inductor, 0.47μH NOM S.A.T.	3510999	1	DD - 0.47	72259
L3	Inductor, .082	3520018	1	551-5172-08-00	
L4	Part of Board				
L5	Part of Board				
L6	Not Used				
L7	Part of Board				
L8	Inductor, 1μH	3510003	2	DD - 1.00	72259
L9	L8				
Q1 thru Q6	NPN, RF	4710026	6	NE73432B	0000S
Q7	D - MOS FET Switch	4710031	1	SD215	18324
R1	Met Ox, 47, 2%, 1/4 W	4130470	3	C4/2%/47	24546
R2	Prec, 1.82K, 1%, 1/10 W	4051821	1	RN55C182F	81349
R3	Comp, 1K, 5%, 1/4 W	4010102	3	RC07GF102J	81349
R4	Met Ox, 560, 2%, 1/4 W	4130561	1	C4/2%/60	24546
R5	Comp, 10, 5%, 1/4 W	4010100	5	RC07GF100J	81349
R6	Met Ox, 82, 2%, 1/4 W	4130820	2	C4/2%/82	24546
R7	R5				
R8	R1				

A201B IF AMPLIFIER

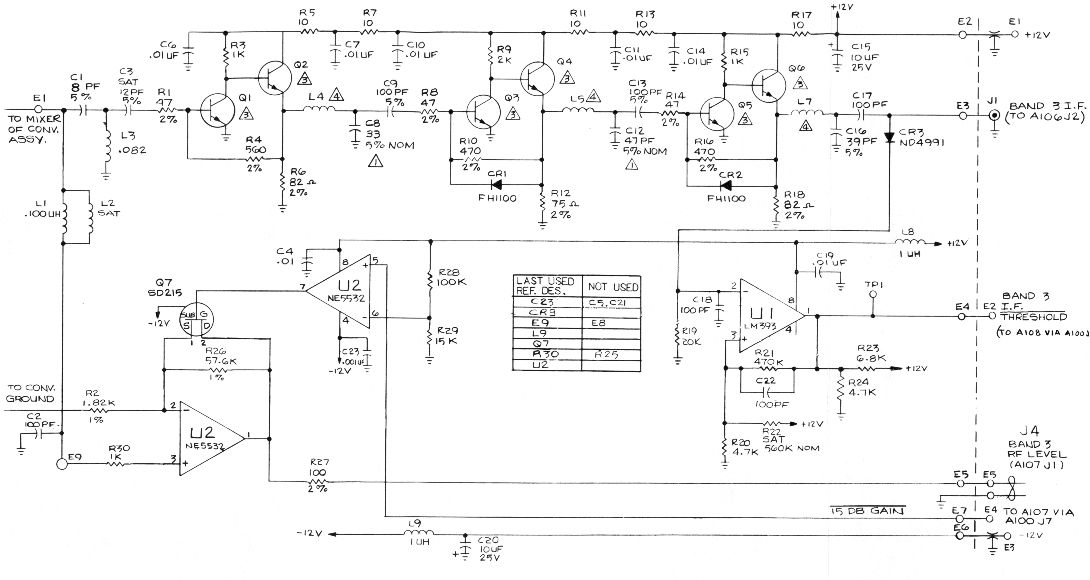
2020143-T

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R9	Comp, 2K, 5%, 1/4 W	4010202	1	RC07GH202J	81349
R10	Met Ox, 470, 2%, 1/4 W	4130471	2	C4/2%/470	24546
R11	R5				
R12	Met Ox, 75, 2%, 1/4 W	4130750	1	C4/2%/75	24546
R13	R5				
R14	R1				
R15	R3				
R16	R10				
R17	R5				
R18	R6				
R19	Comp, 20K, 5%, 1/4 W	4010203	1	RC07GF203J	81349
R20	Comp, 4.7K, 5%, 1/4 W	4010472	2	RC07GF472J	81349
R21	Comp, 470K, 5%, 1/4 W	4010474	1	RC07GF474J	81349
R22	Comp, S.A.T., 5%, 1/4 W	4010999	1	RC07GF564J	81349
R23	Comp, 6.8K, 5%, 1/4W	4010682	1	RC07GF682J	81349
R24	R20				
R25	Not Used				
R26	Pred, 56.6K,1%, 1/10 W	4055762	1	RN55C5762F	81349
R27	Met Ox, 100, 2%, 1/4 W	4130101	1	C4/2%/100	24546
R28	Comp, 100K, 5%, 1/4 W	4010104	1	RC07GF104J	81349
R29	Comp, 15K, 5%, 1/4 W	4010153	1	RC07GF153J	81349
R30	R3				
U1	Dual Comp, Low Power	3050393	1	LM393	0000X
U2	Dual Op Amp.	3045532	1	NE5532	0000X


R5
C7
R7
C10
R9
R11
C11
R13
R15
C14
R17
C15
R18
C16
C17
L7
R3
C6
R6
L3
Q1
Q2
L4
C8
Q3
Q4
R12
L5
C12
Q5
Q6
R4
C9
R8
CR1
R10
C13
R14
CR2
R16
C1
C3
R1
C4
R21
C22
C18
CR3
R28
R29
C23
R23
R24
L1
L2
R30
R2
U2
Q7
C5
L9
R20
R22
U1
C19
L8
R19
C2
R26
R27
C20

2020143 - T

Figure 201B-2. IF Amplifier Component Locator


E1
TO MIXER OF CONV. ASSY.
C1 8 PF 5%
C3 SAT 12PF 5%
L3 .082
R1 47 2%
L1 .100UH
L2 SAT
C6 .01UF
R3 1K
Q1 3
Q2 3
R4 560 2%
R6 82 Ω 2%
R5 10
R7 10
C7 .01UF
C10 .01UF
L4 4
C8 33 5% NOM 1
C9 100PF 5%
R8 47 2%
R9 2K
Q3 3
Q4 3
R10 470 2%
CR1 FH1100
R12 75 Ω 2%
R11 10
R13 10
C11 .01UF
C14 .01UF
L5 4
C13 100PF 5%
R14 47 2%
C12 47PF 5% NOM 1
R15 1K
Q5 3
Q6 3
R16 470 2%
CR2 FH1100
R18 82 Ω 2%
R17 10
+12V
C15 10UF 25V
L7 4
C17 100PF
C16 39PF 5%
CR3 ND4991
E2
E1
+12V
E3
J1
BAND 3 I.F. (TO A106J2)
L8 1 UH
+12V
C4 .01
U2 NE5532
R28 100K
R29 15K
C23 .001UF
-12V
Q7 SD215
SUB G S D
-12V
R26 57.6K 1%
TO CONV. GROUND
R2 1.82K 1%
C2 100PF
E9
R30 1K
U2 NE5532
R27 100 2%
C18 100PF
R19 20K
U1 LM393
C19 .01UF
TP1
E4
E2
BAND 3 I.F. THRESHOLD (TO A108 VIA A100J7)
R21 470K
C22 100PF
R23 6.8K
+12V
R24 4.7K
R22 SAT 560K NOM
+12V
R20 4.7K
J4 BAND 3 RF LEVEL (A107 J1)
E5
E5
15 DB GAIN
E7
E4
TO A107 VIA A100 J7
E6
-12V
E3
L9 1UH
-12V
C20 10UF 25V

LAST USED REF. DES.	NOT USED
C23	C5, C21
CR3	
E9	E8
L9	
Q7	
R30	R25
U2	

4 L4, L5 & L7 ARE PART OF P.C.B.

3 Q1-Q6, 4710026-02 ARE GRADED XSTR PER PROCEDURE 5542002.

1 FACTORY SELECT, NOM VALUE SHOWN.

5500143 - T

Figure 201B-3. IF Amplifier Schematic

Section 10
Options

Section 10 provides descriptions, specifications (where applicable), schematic diagrams and component locators for the options available for use with the Model 545A or 548A Counter.

OPTION

01 D TO A CONVERTER

DAC will convert any three consecutively displayed digits into an analog voltage output on rear panel.

02 POWER MEASUREMENT

1 to 18/26.5 GHz will measure sine wave amplitude to 0.1 dBm resolution and display simultaneously with frequency.
Power offset to 0.1 dB resolution, selectable from front panel.
Option will not degrade the basic performance of the counter.

03 TIME BASE OSCILLATOR $< 5 \times 10^{-9}$ (2010143-03).

04 TIME BASE OSCILLATOR $< 1 \times 10^{-9}$ (2010143-04).

05 TIME BASE OSCILLATOR $< 5 \times 10^{-10}$ (2010143-05).

06 EXTENDED FREQUENCY CAPABILITY - 548A
Use in conjunction with model 590 Frequency Extension Cable Kit
and optional Remote Sensors models 91 thru 94.

07 REMOTE PROGRAMMING/BCD output

08 GENERAL PURPOSE INTERFACE BUS (GPIB)

09 REAR PANEL INPUT

10 CHASSIS SLIDES

OPTION 01
DIGITAL TO ANALOG CONVERTER

Option 01 will convert three consecutive digits to an analog voltage, available on the rear panel. The output will reflect the display, and substitute zeros for any non-numeric characters that appear. The output will be updated after every display update.

SPECIFICATIONS

Output Voltage	0.000 volts to 0.999 volts
Accuracy (25° C)	± 0.5 % ±1 mV
Temp. Stability (0-50° C)	± 0.01 % / °C
Resolution	1 mV
Load Impedance	1 K ohm minimum
Connector	BNC female (on rear panel)
Protection	± 10 V AC or DC applied to output connector will not cause damage. No damage will occur by any load.

OPERATION

On power up the DAC is in off state.

LOCAL OPERATION WITH KEYBOARD

A three key sequence selects the location of the three digits desired, by entering the most significant digit wanted. Digits are numbered 01 through 12.

PRESS : DAC ☐ [X] [X] XX can vary from 01 to 12.

EXAMPLES :

DAC ☐ [0] [1] 1 Hz digit selected

DAC ☐ [0] [2] 10 Hz, 1 Hz digits selected

DAC ☐ [0] [3] 100 Hz, 10 Hz, 1 Hz digits

DAC ☐ [0] [4] 1 kHz, 100 Hz, 10 Hz digits

•
•
•

DAC ☐ [1] [2] 100 GHz, 10 GHz, 1 GHz digits

After pressing DAC ☐ , the display will show the present DAC status, like DAC OFF or DAC XX, and three decimal points will show the locations of the currently selected digits (if DAC is on).

After pressing the first X , the display will show the temporary entry, like DAC X , but the three decimal points will still show the previous DAC status.

After pressing the second X , the display will show the new entry, like DAC X X , and the three decimal points will move to the new places. The DAC output will start to be updated accordingly. Release of the button pressed will return the display back to normal frequency display.

Any wrong key pressed will result in displaying ERROR 10. The operator must restart the key sequence to enter the correct data.

To clear display from DAC data, ERROR display, or ignoring half-sequence entered, press CLEAR ☐ DISPLAY. Display will return to normal and DAC status will not be changed.

To shut off DAC press DAC ☐ DATA ☐ CLEAR or DAC ☐ 0 0

REMOTE OPERATION

For remote operation through GPIB refer to the GPIB (Option 08) section of this manual.

For remote operation through BCD/RMT refer to the BCD/RMT (Option 07) section of this manual.

THEORY OF OPERATION

A simplified block diagram of the DAC board is shown in figure 01-1.

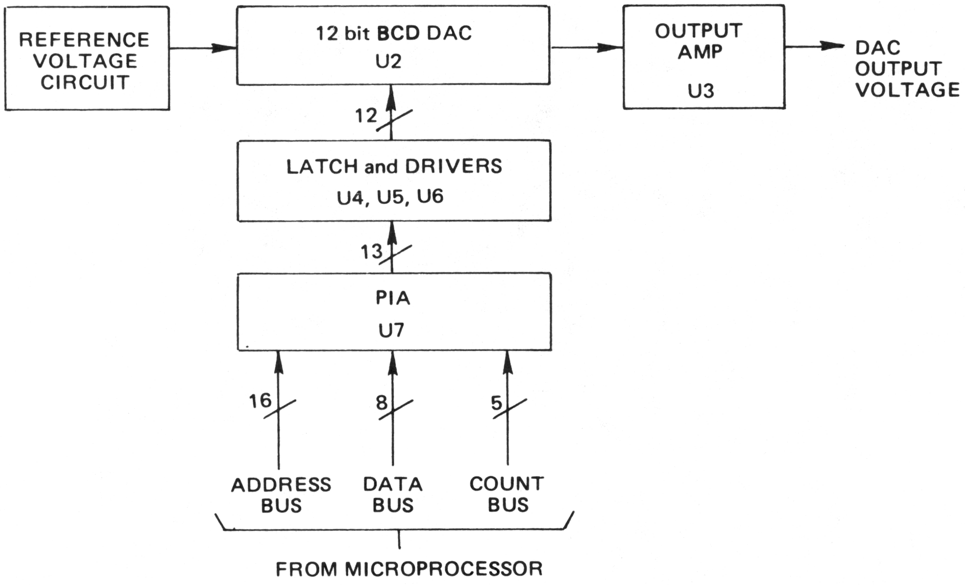

REFERENCE VOLTAGE CIRCUIT
12 bit BCD DAC U2
OUTPUT AMP U3
DAC OUTPUT VOLTAGE
12
LATCH and DRIVERS U4, U5, U6
13
PIA U7
16
8
5
ADDRESS BUS
DATA BUS
COUNT BUS
FROM MICROPROCESSOR

Figure 01-1. DAC Board, Simplified

HARDWARE

PIA AND LATCH DRIVER BLOCKS

The three selected digits are manipulated by the program and sent to the PIA. First the two LSD's are sent to port A, then the third digit (MSD) plus a positive-going pluse (on pin 14 of U7) that triggers the latch U6 so that the complete 12 bit word appears to the DAC inputs (U2). U4 and U5 are level translators from T^2L to CMOS for the DAC.

ANALOG BLOCKS

The DAC is referenced to a 1 volt reference voltage that is generated by CR1 zener and U1 Operational Amplifier. Gain adjustment is provided to calibrate the reference voltage. The DAC U2 converts the 12 bit digital inputs to an analog voltage (0.000V – 0.999V). The output amplifier U3 provides the necessary I/V conversion, output isolation and protection. Zero offset adjustment is provided for calibration purposes, also.

SOFTWARE

The DAC software is described in figures 01-2 and 01-3.

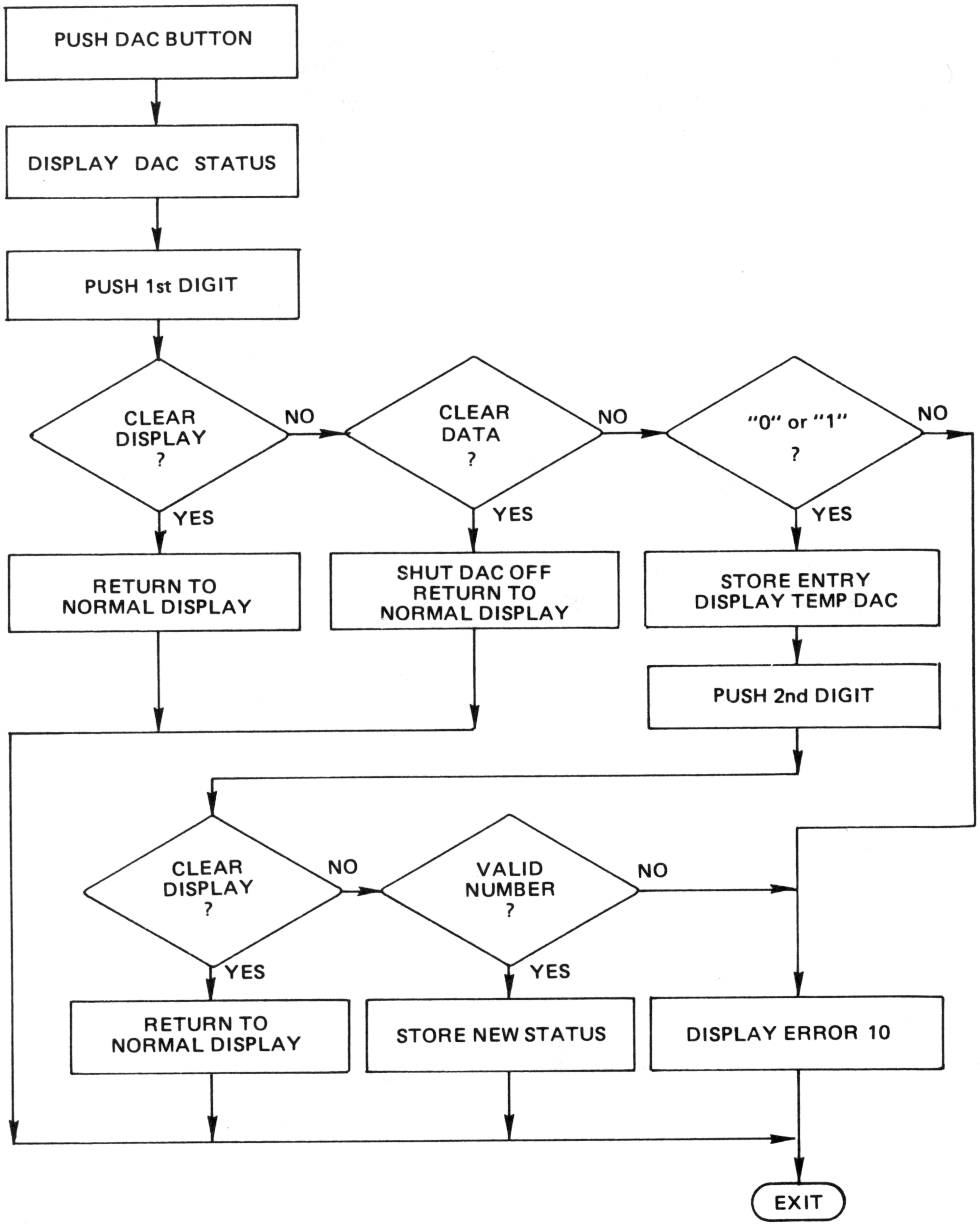

PUSH DAC BUTTON
DISPLAY DAC STATUS
PUSH 1st DIGIT
CLEAR DISPLAY ?
NO
YES
CLEAR DATA ?
NO
YES
"0" or "1" ?
NO
YES
RETURN TO NORMAL DISPLAY
SHUT DAC OFF RETURN TO NORMAL DISPLAY
STORE ENTRY DISPLAY TEMP DAC
PUSH 2nd DIGIT
CLEAR DISPLAY ?
NO
YES
VALID NUMBER ?
NO
YES
RETURN TO NORMAL DISPLAY
STORE NEW STATUS
DISPLAY ERROR 10
EXIT

Figure 01-2. Keyboard Control

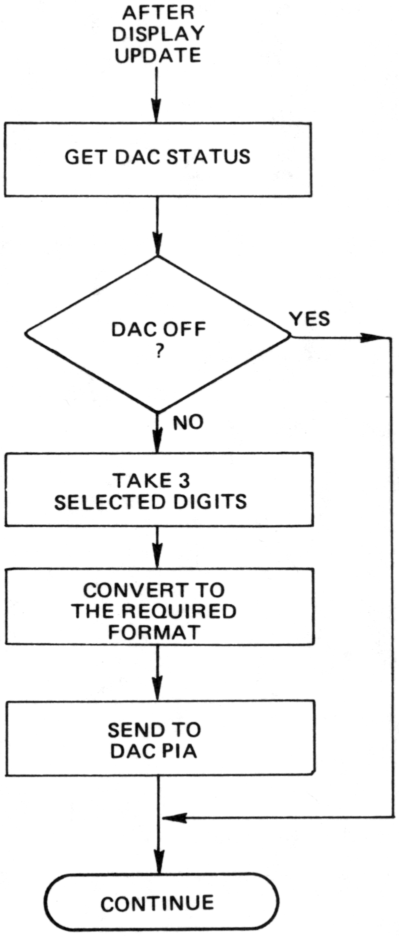

AFTER
DISPLAY
UPDATE
GET DAC STATUS
DAC OFF
?
YES
NO
TAKE 3
SELECTED DIGITS
CONVERT TO
THE REQUIRED
FORMAT
SEND TO
DAC PIA
CONTINUE

Figure 01-3. DAC Board Update

CALIBRATION

The following instruments or their equivalents are required to perform calibration of the DAC board. Calibration is required every six months or after the board has been repaired.

BRAND	MODEL	TYPE	SPECIFICATIONS
Fluke	8050A	DVM	4 ½ digit resolution

ZERO OFFSET CALIBRATION

1. Turn on the counter with no input, so that the display shows all zeros.
2. PUSH DAC 0 3
3. Connect digital volt meter to the rear DAC output.
4. Adjust R6 to reach 0.000 volts on the DVM display.

FULL SCALE CALIBRATION

1. Short TP3 to TP4.
2. Adjust R4 to reach 1.000 volts on the DVM display.
3. Remove the short.

The calibration for the DAC board is complete.

PERFORMANCE TESTS

Refer to the instruments table in Calibration for the required test equipment.

Connect the DVM to the DAC output (rear panel). Connect rear 10 MHz output to Band 1 input.

ENTER : BAND 1 RESOL 2 Display shows 10.000 0 MHz.

ACCURACY TEST

ENTER : DAC 0 6 DVM should read 0±1mV.

ENTER : FREQ OFFSET • 9 9 9 MHz DVM should read 0.999±0.006 V.

Repeat the second test in accuracy for entries between .888 and .111. DVM should read the entry ± 1 mV ± 0.5 % of entry.

TROUBLESHOOTING

1. If zero offset calibration cannot be achieved check that all digital inputs to U2 (pins 3 to 15) are at "low" levels (< + 0.5 V). If they are , try to replace U2 or U3.

2. If full scale calibration cannot be achieved check that there is 6.2 volts at TP1. If voltage is wrong, replace CR1 or R1 after verifying the + 12 V supply. If the voltage at TP1 is correct check TP2. The voltage at TP2 should read 1.000 volts. If wrong the failure is in U1 or the resistors R2, R3 or R4. If still wrong replace U2.

3. The digital lines in the DAC board can be checked in three ways.

   - A static test by connecting the rear time base 10 MHz output to Band 1 input.

     ENTER : [BAND] [1] [RESOL] [2] Display shows 10.000 0 MHz

     ENTER : [DAC] [0] [6]

     Now entering [FREQ OFFSET] [•] [X] [X] [X] [MHz] will cause a display of 10.XXX0 MHz.

     The XXX are selected to the DAC board, so the three BCD's should appear on U7, pins 2 to 13 (pin 2 is the LSB). On pin 14 there should be positive pulses. Checking two combinations like 777 and 888 can locate a fault in the digital path between U7 outputs and U2 inputs.

   - A dynamic test that is provided with the DAC option.

     ENTER : [TEST] [1] [1]

     A continuous count ramp from 000 to 999 is sent to the DAC board, regardless of DAC status or display.

     Connect the DAC rear output to an oscilloscope. A ramp should be observed going from 0 to .999 volts. The ramp is built with 1 mV amplitude steps. Any failure in one or more digital lines in the board will cause either breaking in the ramp or a multiple amplitude steps (2mV, 4 mV, ect.). Careful analysis will show the bad line or lines.

   - By Signature analysis while operating in the dynamic test just described, and checking the following signatures.

DAC OPTION SIGNATURES

	START	STOP	CLOCK
CONNECTIONS	A106 TP5	A106 TP5	A105 TP8
BUTTONS	OUT ↑	IN ↓	IN ↓

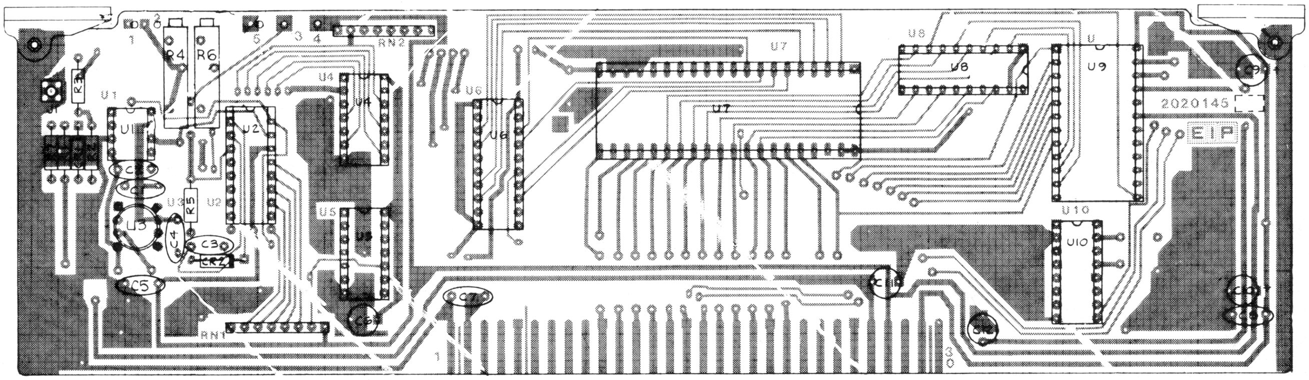
LINE	SIGNATURE
U4 pin — 2	46F0
4	79HH
6	7U60
8	4F30
10	9115
12	17HP
+5 V	1915
U5 pin — 2	2597
4	7P0U
6	U8A9
8	P1C0
10	7808
12	7C4C
U6 pin — 2	2597
5	7P0U
6	U8A9
9	P1C0
12	7808
15	7C4C
16	46F0
19	79HH

LINE	SIGNATURE
+5 V	1915
U7 pin — 2	0F91
3	7F31
4	4CA3
5	3241
6	U738
7	5UPU
8	0659
9	5HHF
10	7U60
11	4F30
12	9115
13	17HP
14	30UC

OPTION 01 – DIGITAL TO ANALOG CONVERTER

2020145 - H

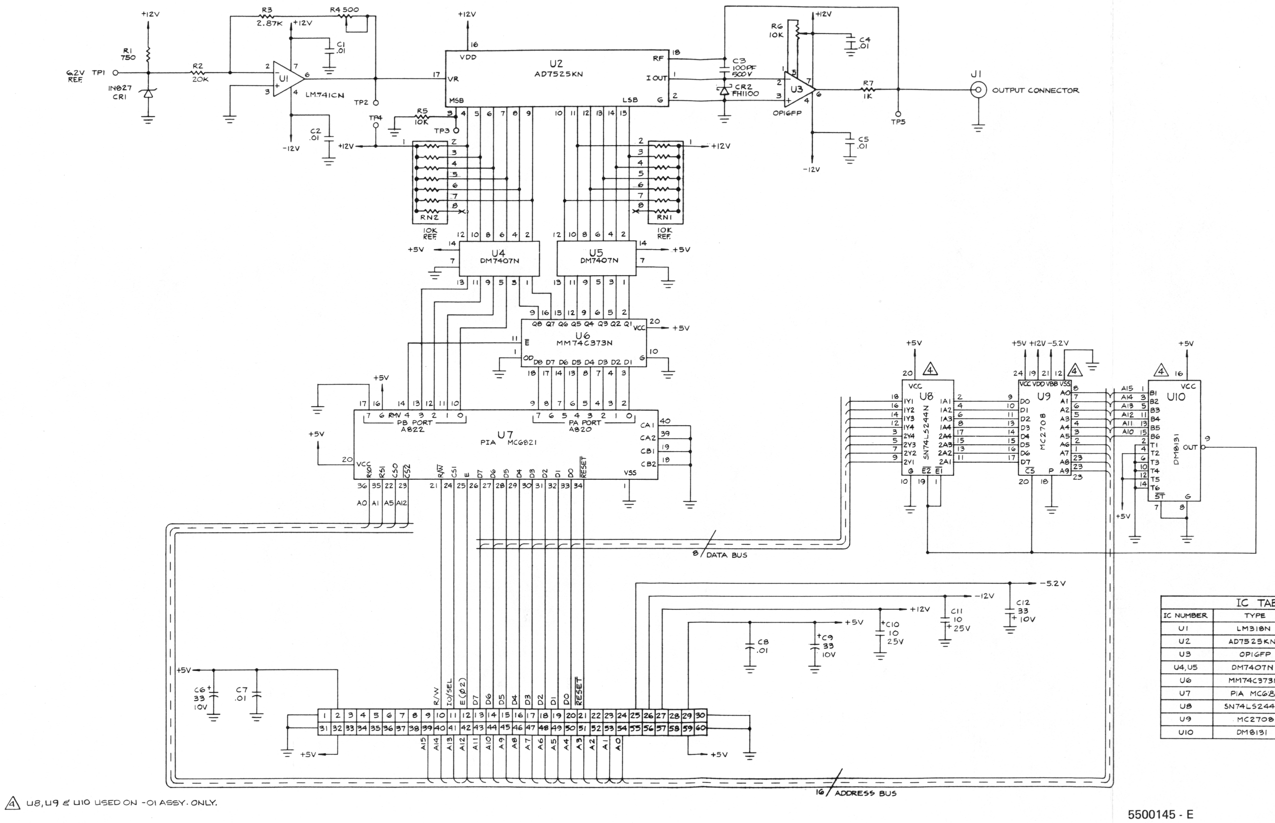
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A104	Digital to Analog Converter Assy	2020145-02	Ref.	EIP	
C1	Cer, .01 μ F, 20%, 100V	2150003	6	TG-S10	56289
C2	C1				
C3	Mica, 100pF, 5%, 500V	2260034	1	CD10FD101J03	56289
C4	C1				
C5	C1				
C6	Tant, 33 μ F, 20%, 10V	2300015	3	TAG20-33/10-50	14433
C7	C1				
C8	C1				
C9	C6				
C10	Tant, 10 μF, 20%, 25V	2300029	2	TAG20-10/25-20	14433
C11	C10				
C12	C6				
CR1	Zener, 6.2V	2700827	1	IN827	
CR2	Shottky, Barrier	2710004	1	FH1100	07263
R1	Comp, 750, 5%, ¼ W	4010751	1	RC07GF751J	81349
R2	Prec, 20K, 1%, ¼W	4052002	1	RN55C32002F	81349
R3	Prec, 2.87K, 1%, ¼W	4062871	1	RN55C6191F	81349
R4	Variable, 500 ohm	4280009	1	89PR500	
R5	Comp, 10K, 5%, ¼ W	4010103	1	RC07GF103J	81349
R6	Variable, 10K ohm	4280006	1	89PR10K	
R7	Comp, 1K, 5%, ¼ W	4010102	1	RC07GF102J	81349
RN1	Network of 7,10K	4170004	2	4308R-101-103	32997
RN2	RN1				
U1	Op Amplifier	3040741	1	LM741N	0000X
U2	DAC	3050752	1	AD7525KN	0000X
U3	Prec, Op Amplifier, JFET	3041016	1	OP16FP	06665
U4	Hex Buffer	3007404	2	DM7407N	0000X
U5	U4				
U6	8 Bit Latch	3034373	1	MM74C373N	
U7	PIA	3086820	1	MC6821	04731
U8	Oct. Driver	3084244	1	SN74LS244N	01295
U9	Program PROM 9	6400001-09	1	TM2708	01295
U10	6 Bit Comparitor	3078131	1	DM8131	0000X


1
2
R4
R6
R3
5
3
4
RN2
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
R5
C3
C4
C5
CR2
C7
RN1
1
30
2020145
EIP

U8, U9, U10 are not used in models 545A/548A

2020145 - H

Figure 01-4. DAC Component Locator


U1 LM741CN
U2 AD7525KN
U3 OP16FP
U4 DM7407N
U5 DM7407N
U6 MM74C373N
U7 PIA MC6821
U8 SN74LS244N
U9 MC2708
U10 DM8131
6.2V REF
TP1
TP2
TP3
TP4
TP5
R1 750
R2 20K
R3 2.87K
R4 500
R5 10K
R6 10K
R7 1K
1N827 CR1
CR2 FH1100
C3 100PF 500V
RN1 10K REF.
RN2 10K REF.
J1 OUTPUT CONNECTOR
PB PORT A822
PA PORT A820
8 DATA BUS
16 ADDRESS BUS
+12V
-12V
+5V
-5.2V
C6 33 10V
C7 .01
C8 .01
C9 33 10V
C10 10 25V
C11 10 25V
C12 33 10V
4 U8, U9 & U10 USED ON -01 ASSY. ONLY.

IC TABLE		PIN NO.				
IC NUMBER	TYPE	GND	+12	-12	+5	-5.2
U1	LM318N	3	7	4		
U2	AD7525KN	2	16			
U3	OP16FP	3	7	4		
U4, U5	DM7407N	7			14	
U6	MM74C373N	10			20	
U7	PIA MC6821	1			20	
U8	SN74LS244N	10			20	
U9	MC2708	18	19		24	21
U10	DM8131	8			16	

5500145 - E

Figure 01-5. DAC Schematic

OPTION 02
POWER MEASUREMENT

Option 02 measures the power of signals applied to Band 3. The power is displayed (to 0.1 dB resolution) simultaneously with frequency (to 100 kHz max. resolution). For A.M. and F.M. averaging purposes, gate time is controllable in the power meter mode, through the resolution function. Power gate time mirrors frequency gate time. For example, in resolution 0 the frequency gate time is 1 second, and the power gate time is 1 second. In resolution 1 the frequency gate time is 100 msec., and the power gate time is 100 msec. Option 02 allows power offsets from -99.9 dB to 99.9 dB, with a 0.1 dB resolution and will not degrade the basic performance of the counter.

SPECIFICATIONS

ACCURACY	± 1.2 dB Typical 0-50° C ± 0.5 dB Typical 25° C
TIME ADDED	1 GATE TIME + 50 msec.
RESOLUTION	0.1 dB POWER, Selectable 100 kHz - 1 GHz Frequency
RANGE	ENTIRE OPERATING RANGE OF BAND 3

OPERATION

To turn the power meter on press: **POWER METER on/off** ☐

If the counter is displaying only frequency it will begin displaying frequency and power. If the counter is displaying frequency and power it will begin displaying frequency only.

Turn the power meter on. Observe the display. Frequency is displayed on the left, and power is displayed on the right. The POWER dBm annunciator lights to indicate power meter operation. If the signal is too small to measure the power, the display will show EE.E in the power meter digits. (Since 0 dBm is a valid power, 00.0 can not be used as a no power indicator.)

Power meter offsets are entered and displayed in the same manner as other data. Refer to the Display and Data Entry Sequence in Section 3.

To turn the power meter off press: **POWER METER on/off** ☐

THEORY OF OPERATION

The power meter uses the Schottky diode in the microwave converter as its power sensor. The output of the diode detector is connected to a programmable gain attenuator, which consists of two switchable gain stages (one is in the IF Amplifier A201B and one is on the Gate Generator A107) and two 8 bit attenuators. A comparitor, set to 100 mV, and a TTL latch provide output information to the microprocessor. See figure 02-1.

After the counter has a signal, and has taken a frequency reading, it starts the power meter task. This triggers the gate time counter, resets the TTL power latch, moves the yig ±50 MHz (to insure that the signal peak is passed through), then checks the TTL power latch. If the latch is set, the attenuation is increased in 3 dB steps (until the signal is attenuated below the level of the comparitor), then back one step. If maximum attenuation is reached, and the latch is still being set, the word OVERLOAD is displayed and the task is exited.

When the latch is first checked, if it is still reset, the attenuation is decreased in 3 dB steps until the comparator level is reached. If minimum attenuation (maximum gain) is reached, the display is set to EE.E, and the task is exited.

After the attenuation is adjusted to a 3 dB resolution a successive approximation is performed to find the attenuation to a 0.1 dB resolution. The attenuation is stored, and if the gate time counter is not finished, the cycle is repeated. When the gate time counter is finished all the readings are averaged to eliminate the effects of AM on the signal.

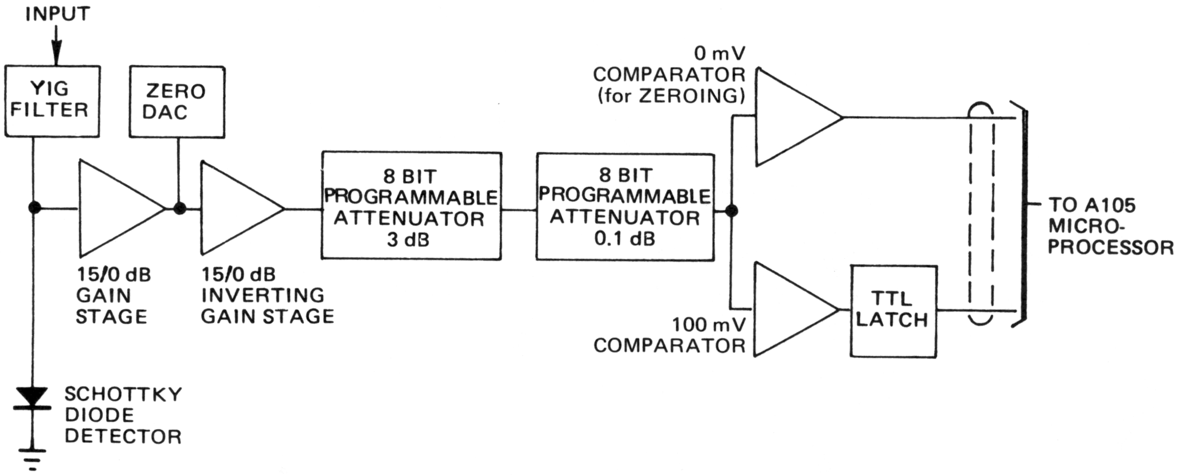

INPUT
YIG FILTER
ZERO DAC
15/0 dB GAIN STAGE
15/0 dB INVERTING GAIN STAGE
8 BIT PROGRAMMABLE ATTENUATOR 3 dB
8 BIT PROGRAMMABLE ATTENUATOR 0.1 dB
0 mV COMPARATOR (for ZEROING)
100 mV COMPARATOR
TTL LATCH
TO A105 MICRO-PROCESSOR
SCHOTTKY DIODE DETECTOR

Figure 02-1. Power Meter Hardware

The "power vs power" and "power vs frequency" corrections are added, and the sum is displayed. A detailed flowchart of the power meter is shown is figure 02-2.

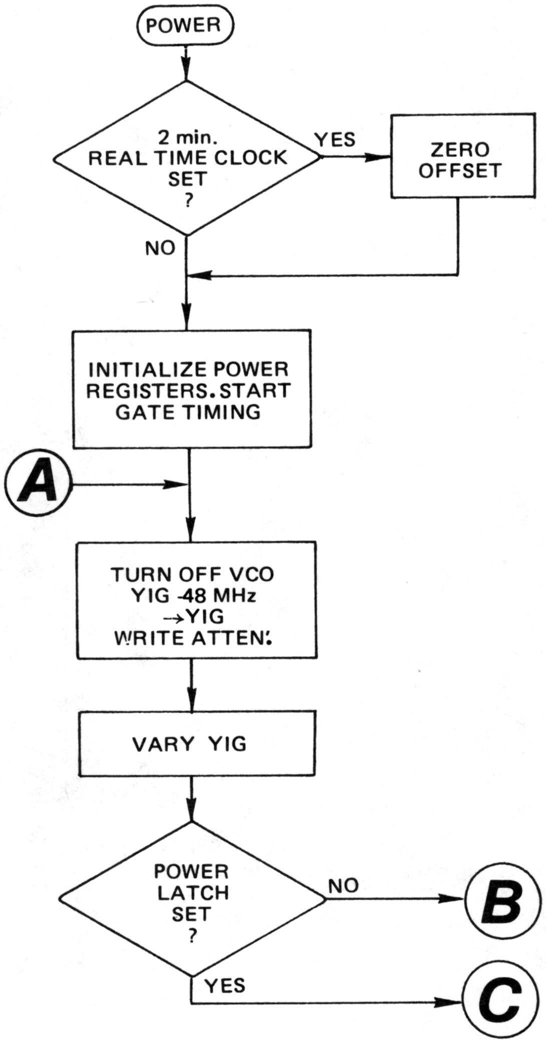

POWER
2 min.
REAL TIME CLOCK
SET
?
YES
ZERO
OFFSET
NO
INITIALIZE POWER
REGISTERS. START
GATE TIMING
A
TURN OFF VCO
YIG -48 MHz
→YIG
WRITE ATTEN.
VARY YIG
POWER
LATCH
SET
?
NO
B
YES
C

Figure 02-2. Power Meter Task

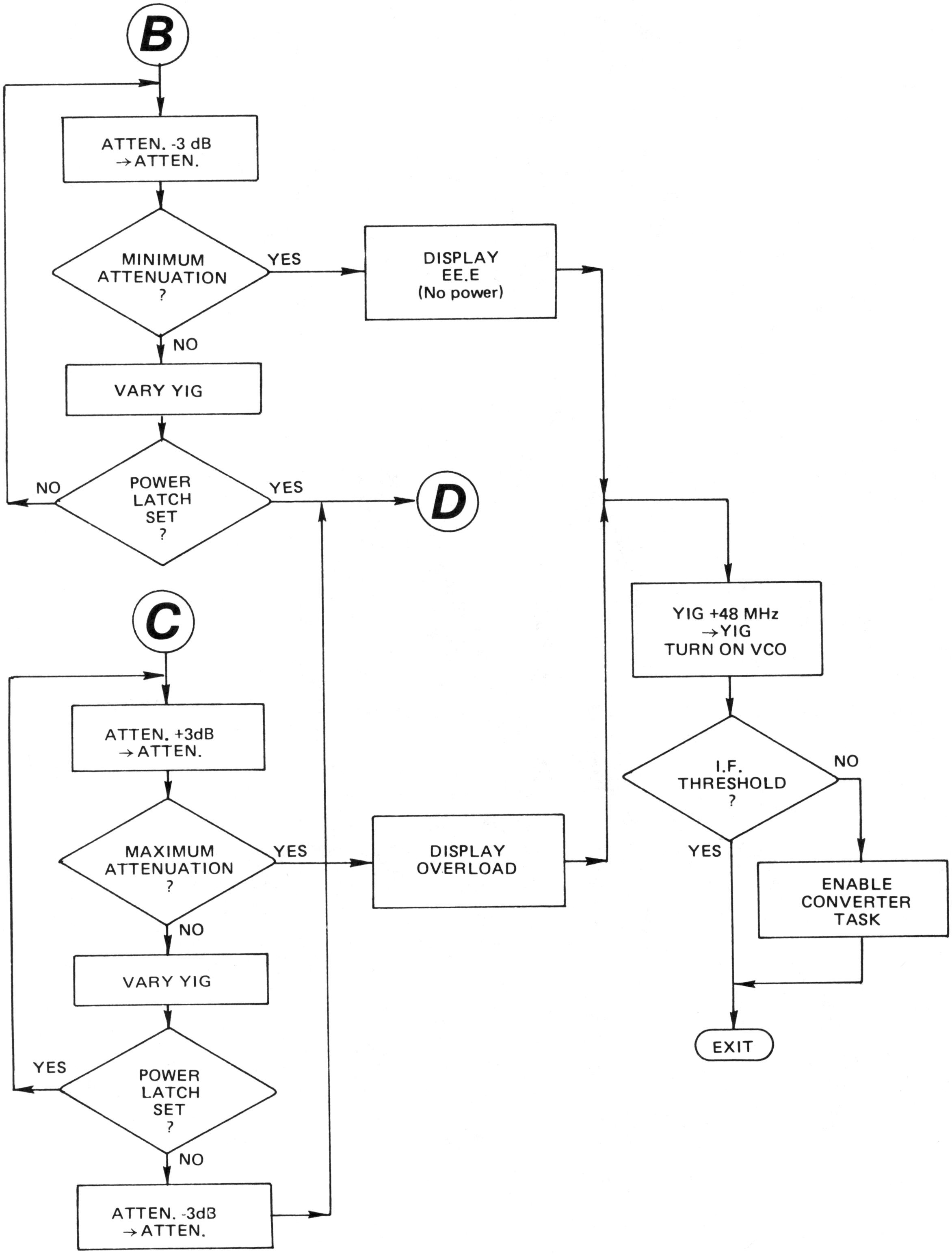

B
ATTEN. -3 dB
→ATTEN.
MINIMUM ATTENUATION ?
YES
DISPLAY EE.E (No power)
NO
VARY YIG
POWER LATCH SET ?
NO
YES
D
C
ATTEN. +3dB
→ATTEN.
MAXIMUM ATTENUATION ?
YES
DISPLAY OVERLOAD
NO
VARY YIG
POWER LATCH SET ?
YES
NO
ATTEN. -3dB
→ATTEN.
YIG +48 MHz
→YIG
TURN ON VCO
I.F. THRESHOLD ?
NO
YES
ENABLE CONVERTER TASK
EXIT

Figure 02-2. Power Meter Task, continued

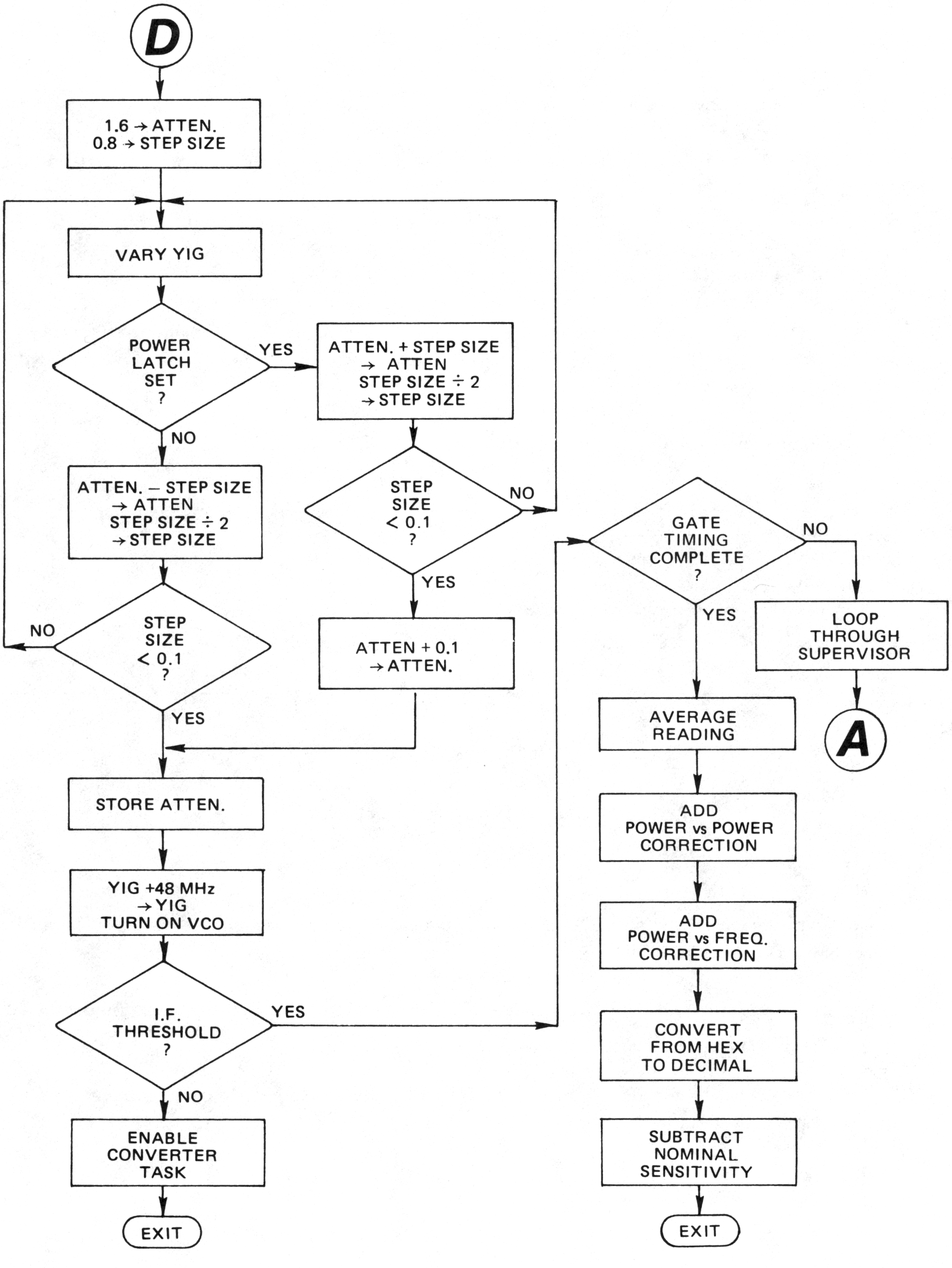

D
1.6 → ATTEN.
0.8 → STEP SIZE
VARY YIG
POWER LATCH SET ?
YES
ATTEN. + STEP SIZE → ATTEN
STEP SIZE ÷ 2 → STEP SIZE
NO
ATTEN. – STEP SIZE → ATTEN
STEP SIZE ÷ 2 → STEP SIZE
STEP SIZE < 0.1 ?
NO
YES
ATTEN + 0.1 → ATTEN.
STEP SIZE < 0.1 ?
NO
YES
STORE ATTEN.
YIG +48 MHz → YIG
TURN ON VCO
I.F. THRESHOLD ?
YES
NO
ENABLE CONVERTER TASK
EXIT
GATE TIMING COMPLETE ?
NO
YES
LOOP THROUGH SUPERVISOR
A
AVERAGE READING
ADD POWER vs POWER CORRECTION
ADD POWER vs FREQ. CORRECTION
CONVERT FROM HEX TO DECIMAL
SUBTRACT NOMINAL SENSITIVITY
EXIT

Figure 02-2. Power Meter Task, continued

CALIBRATION

The power meter contains 690 correction factors, stored in PROM.

The 150 "power vs power" correction factors compensate for variations from square law in the detector and power meter circuits. They are divided into three tables. The first table corrects variations below 10 GHz. The second corrects variations between 10 and 20 GHz. The third corrects variations above 20 GHz.

The 540 "power vs frequency" correction factors compensate for variations in the detector output at different frequencies. "Power vs frequency" corrections cover 0-27 GHz every 50 MHz.

The power meter is calibrated at the factory using specialized automatic test equipment. Because of the accuracy required, recalibration in the field is not recommended. If, however, recalibration is required, use the procedures given herein.

The test equipment required for calibration is:

MFG	MODEL	DESCRIPTION	CRITICAL PARAMETERS
H.P.	435A	Power Meter	Measures -30 to +15 dBm
Wavetek	2002	Sweeper	950 MHz - 2 GHz
Wiltron	6100	Microwave Sweeper	2 GHz - 18 GHz
Wiltron	6100	Microwave Sweeper	18 GHz - 26.5 GHz
E.H.		PROM Programmer	Programs TI 2516 PROMS

CAUTION

Be sure all connections are clean
and tight. Loose or dirty connections
will cause calibration errors.

1. Duplicate the power meter PROM, zeroing all corrections (address 0000-02B2 in the PROM). Install the uncorrected PROM in the counter.
2. Set the Wavetek to 2 GHz ±1 MHz. Connect the Wavetek to band 3 of the counter. Adjust the output until the counter reads -35 dBm.
3. Connect Wavetek to the power meter. Subtract the counter reading from the power meter reading. Round the result (R_1) to 0.1 dBm.
4. Using the following formulas, justify the correction to a number between 10 and 20.

$$\text{int}(R_1) - 1 = N \; ; \; (\text{int}(R_1) = \text{Whole number portion of } R_1)$$

$$10(R_1 - N) = CORR_{10}$$

$$\text{Convert } CORR_{10} \text{(decimal)} \rightarrow CORR_{16} \text{ (hexidecimal)}$$

(R_1 is the result of step 3.)

5. Program the correction in these locations.

   0000 - 0005 inclusive
   0032 - 0037 inclusive
   0064 - 0069 inclusive

6. Connect the Wavetek to the counter. Increase power until the counter reads 1 dB higher.

7. Connect the Wavetek to the power meter. Subtract the counter reading from the power meter reading. Round the result (R_2) to 0.1 dBm.

8. Using the following formulas, calculate the correction.

   $$10\,(R_2 - N) = \mathrm{CORR}_{10}$$

   $$\text{Convert } \mathrm{CORR}_{10} \rightarrow \mathrm{CORR}_{16}$$

   (R_2 is the result of step 7, and N was found in step 4.)

9. Program the correction in the 3 addresses found by the following formulas.

   $$40 + P = \text{Add } 1_{10},\ \text{Add } 1_{10} \rightarrow \text{Add } 1_{16}$$

   $$40 + P + 50 = \text{Add } 2_{10},\ \text{Add } 2_{10} \rightarrow \text{Add } 2_{16}$$

   $$40 + P + 100 = \text{Add } 3_{10},\ \text{Add } 3_{10} \rightarrow \text{Add } 3_{16}$$

   (P is the power the counter was set at in step 6.)

10. Repeat steps 6 through 9 until overload is reached on the counter.

11. Install the partially corrected PROM in the counter.

12. Set the Wavetek to 950 MHz, about -15 dBm.

13. Measure the power on the counter and power meter. Subtract the counter reading from the power meter reading. Round the results to 0.1 dBm. Multiply the results by 10 and convert to hex.

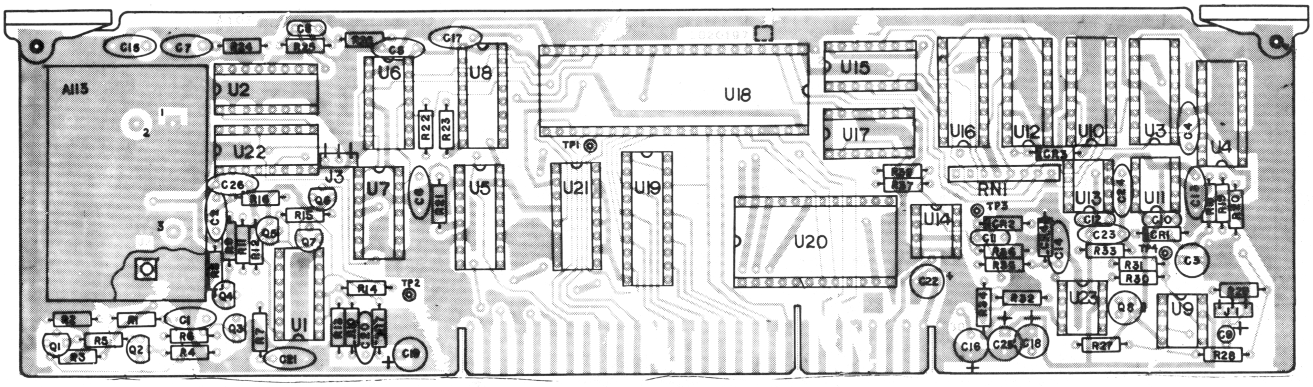
14. Program the correction in the address found by the following formula.

    $$\frac{\text{FREQ (MHz)}}{50} + 150 = \text{Add}_{10}$$

    $$\text{Add}_{10} \rightarrow \text{Add}_{16}$$

15. Increase frequency by 50 MHz. Repeat steps 13 and 14. Adjust the sweepers as necessary, until the upper frequency limit of the counter is reached.

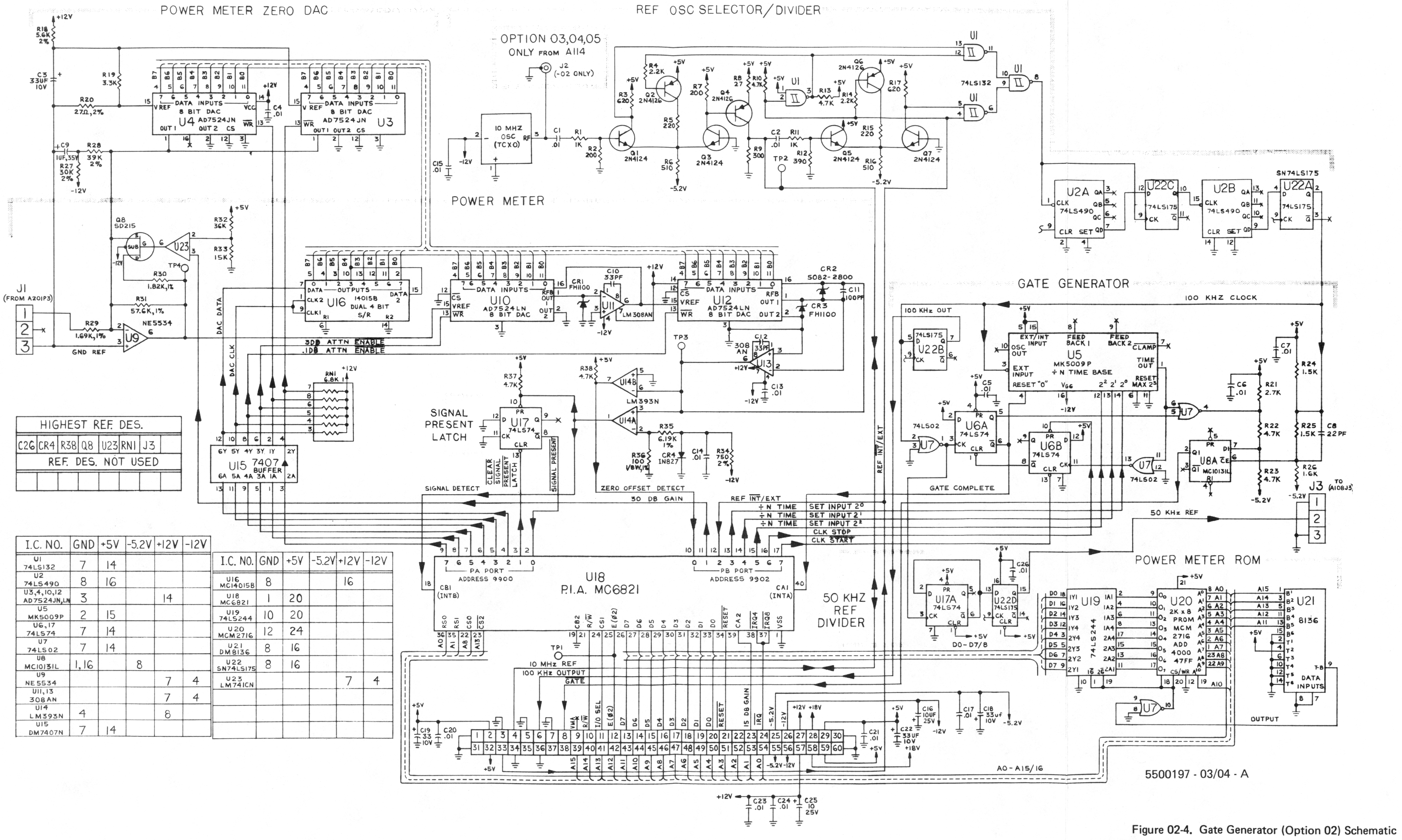
Refer to section 9, pages 107-5 through 107-9, for parts list and schematic diagram. The counter recalibration is now complete.


A115
U2
U22
U6
U8
U18
U15
U17
U16
U12
U10
U3
U4
U7
U5
U21
U19
U20
U14
RN1
U13
U11
U1
U23
U9
J3
J1
TP1
TP2
TP3
TP4
C16
C7
C8
C6
C17
C26
C21
C1
C4
C5
C9
C12
C10
C11
C22
C23
C24
C25
C18
C3
CR1
CR2
CR3
R1
R2
R3
R4
R5
R6
R14
R15
R16
R17
R21
R22
R23
R24
R25
R26
R27
R28
R30
R31
R32
R33
R34
R35
R36
R37
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8

-04	OPT.02/03,04,05	545A/548A
-03	2010225	548A
-03	2010224	545A
DASH NO.	NEXT ASSY	USED ON
	APPLICATION	

2020197 - 03/04 - A

Figure 02-3. Gate Generator (Option 02) Component Locator


POWER METER ZERO DAC
REF OSC SELECTOR/DIVIDER
OPTION 03,04,05 ONLY FROM A114
J2 (-02 ONLY)
10 MHZ OSC (TCXO)
POWER METER
GATE GENERATOR
100 KHZ CLOCK
100 KHz OUT
U4 AD7524JN 8 BIT DAC
U3 AD7524JN 8 BIT DAC
U16 14015B DUAL 4 BIT S/R
U10 AD7524LN 8 BIT DAC
U12 AD7524LN 8 BIT DAC
U11 LM308AN
U13 308AN
U9 NE5534
U23
Q8 SD215
J1 (FROM A201P3)
GND REF
DAC DATA
DAC CLK
3DB ATTN ENABLE
.1DB ATTN ENABLE
U15 7407 BUFFER
RN1 6.8K
SIGNAL PRESENT LATCH
U17 74LS74
U14A
U14B LM393N
SIGNAL DETECT
CLEAR SIGNAL PRESENT LATCH
SIGNAL PRESENT
ZERO OFFSET DETECT
30 DB GAIN
REF INT/EXT
÷ N TIME
SET INPUT 2⁰
SET INPUT 2¹
SET INPUT 2²
CLK STOP
CLK START
U18 P.I.A. MC6821
PA PORT ADDRESS 9900
PB PORT ADDRESS 9902
50 KHZ REF DIVIDER
U5 MK5009P ÷ N TIME BASE
U22B 74LS175
U6A 74LS74
U6B 74LS74
U7 74LS02
U8A MC10131L
GATE COMPLETE
50 KHz REF
J3 TO (A108J5)
U2A 74LS490
U22C 74LS175
U2B 74LS490
U22A SN74LS175
U1 74LS132
POWER METER ROM
U17A 74LS74
U22D 74LS175
U19 74LS244
U20 2K x 8 PROM MCM 2716 ADD 4000 47FF
U21 8136
DATA INPUTS
OUTPUT
D0-D7/8
A0-A15/16
10 MHz REF
100 KHz OUTPUT
GATE
TP1
TP2
TP3
TP4

HIGHEST REF. DES.							
C26	CR4	R38	Q8	U23	RN1	J3	
REF. DES. NOT USED							

I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U1 74LS132	7	14			
U2 74LS490	8	16			
U3,4,10,12 AD7524JN,LN	3			14	
U5 MK5009P	2	15			
U6,17 74LS74	7	14			
U7 74LS02	7	14			
U8 MC10131L	1,16		8		
U9 NE5534				7	4
U11,13 308AN				7	4
U14 LM393N	4			8	
U15 DM7407N	7	14			

I.C. NO.	GND	+5V	-5.2V	+12V	-12V
U16 MC14015B	8			16	
U18 MC6821	1	20			
U19 74LS244	10	20			
U20 MCM2716	12	24			
U21 DM8136	8	16			
U22 SN74LS175	8	16			
U23 LM741CN				7	4

5500197 - 03/04 - A

Figure 02-4. Gate Generator (Option 02) Schematic

OPTIONS 03, 04, 05
TIME BASE OSCILLATORS

Three Time Base Oscillators are available as options for either the model 545A or 548A. These high stability options enhance the accuracy of the counter by the addition of oven stabilized crystal oscillators. These oscillators improve counter operation by reducing both time temperature variations.

When any one of these options is installed, the TCXO is removed from the Gate Generator board (A107) and the following components are added.

- One of three Oven Oscillators (A114) mounted on the chassis.
- 28 VDC Power Supply board (A112), assembly part number 2010226
- Power Supply Transformer T1 (part number 4900006) mounted on A112.
- Time Base Adjustment Pot J2 (part number 2010190) mounted on the rear panel.
- Related interconnecting cable harnesses.

	OPTION 03	OPTION 04	OPTION 05
CHARACTERISTIC	2030010 - 01	2030010 - 02	2030010 - 03
AGING RATE/24 HOURS (After 72 hour warm-up)	$<\|5 \times 10^{-9}\|$	$<\|1 \times 10^{-9}\|$	$<\|5 \times 10^{-10}\|$
SHORT TERM STABILITY (1 second average)	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms	$< 1 \times 10^{-10}$ rms
0° to + 50° C TEMPERATURE STABILITY	$<\|6 \times 10^{-8}\|$	$<\|3 \times 10^{-8}\|$	$<\|3 \times 10^{-8}\|$
± 10% LINE VOLTAGE CHANGE	$<\|5 \times 10^{-10}\|$	$<\|2 \times 10^{-10}\|$	$<\|2 \times 10^{-10}\|$

Figure 03/04/05-1. Time Base Oscillator Option Specifications

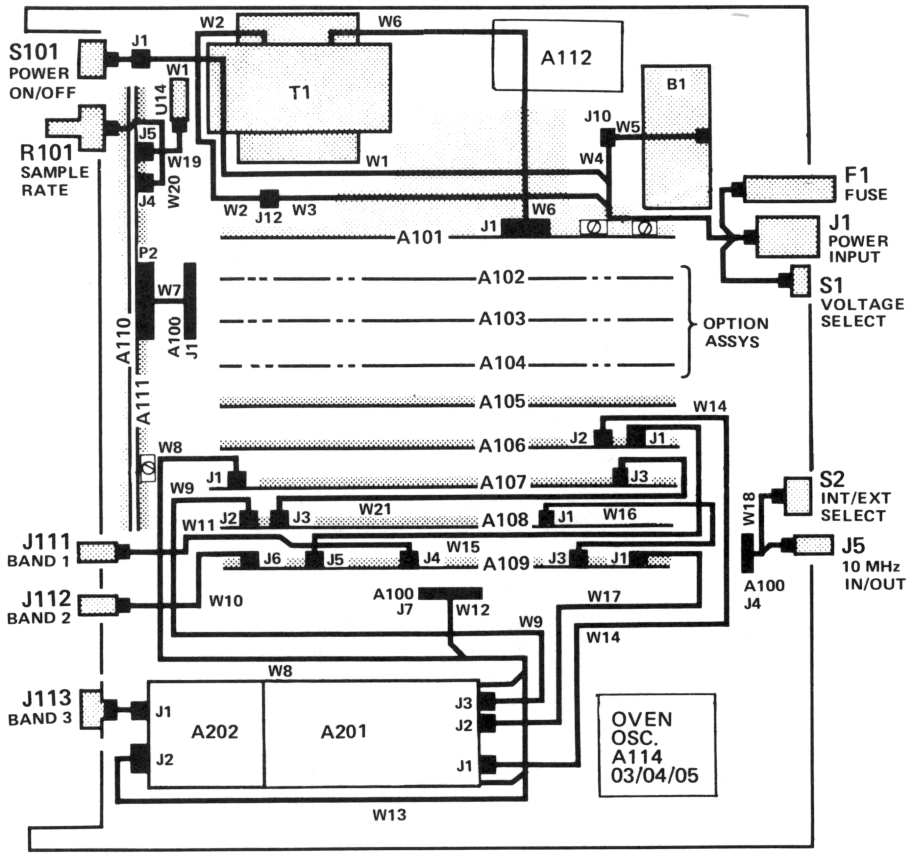

S101
POWER
ON/OFF
R101
SAMPLE
RATE
J1
W2
W6
W1
U14
T1
A112
B1
J10
W5
W4
J5
W19
W20
J4
W1
W2
J12
W3
J1
W6
F1
FUSE
J1
POWER
INPUT
A101
S1
VOLTAGE
SELECT
P2
W7
A102
A103
A104
OPTION
ASSYS
A110
A100
J1
A111
A105
W14
A106
J2
J1
W8
J1
A107
J3
W9
S2
INT/EXT
SELECT
W18
W11
J2
J3
W21
A108
J1
W16
J111
BAND 1
J6
J5
J4
W15
A109
J3
J1
J5
10 MHz
IN/OUT
A100
J4
J112
BAND 2
W10
A100
J7
W12
W17
W9
W14
W8
J113
BAND 3
J1
A202
A201
J3
J2
J2
J1
OVEN
OSC.
A114
03/04/05
W13

Figure 03/04/05-2. Component Location, Time Base Option

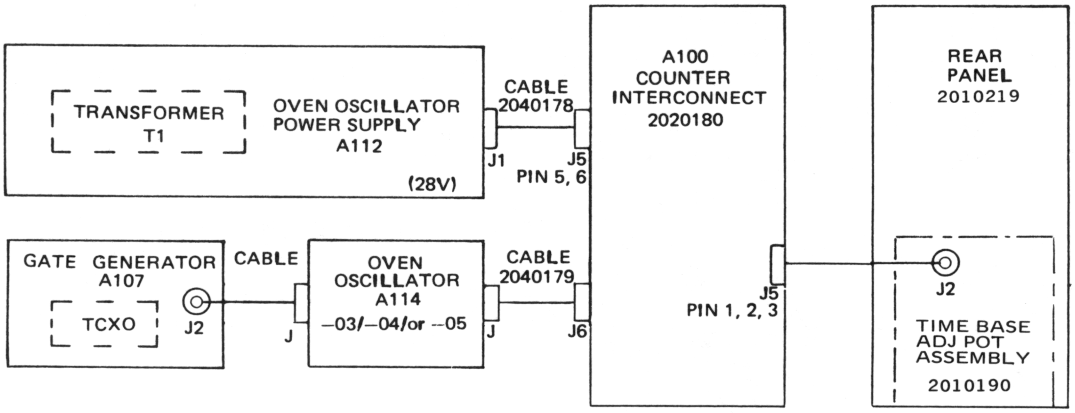

TRANSFORMER
T1
OVEN OSCILLATOR
POWER SUPPLY
A112
(28V)
CABLE
2040178
J1
J5
PIN 5, 6
A100
COUNTER
INTERCONNECT
2020180
REAR
PANEL
2010219
GATE GENERATOR
A107
TCXO
J2
CABLE
J
OVEN
OSCILLATOR
A114
–03/–04/or –05
CABLE
2040179
J
J6
J5
PIN 1, 2, 3
J2
TIME BASE
ADJ POT
ASSEMBLY
2010190

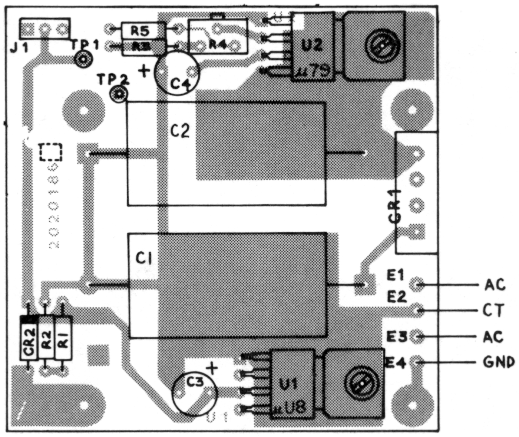
Figure 03/04/05-3. Time Base Option, Interconnection Diagram

OVEN OSCILLATOR POWER SUPPLY

The Oven Oscillator Power Supply board (A112) is a simple 28V regulated, current limited power supply. U1 and U2 provide voltage regulation, thermal protection and current limiting.

The transformer T1, CR1, C1 and C2 provide a 40V nominal unregulated DC voltage. The output voltage is set by voltage divider R5, R3 and R4. These resistors were selected so that 28V out provides 2.23V at U2 pin 2 (to U2 pin 1). Diode CR2 protects the supply from being pulled more negative than ground. See the schematic in figure 03/04/05-6.

The power supply (A112) is on and operating as long as the counter is connected to an active AC power source. The counter's POWER ON/OFF switch on the front panel does not control this assembly.



2020186

Figure 03/04/05-4. Oven Oscillator Power Supply (A112) Component Location

OVEN OSCILLATOR CALIBRATION

When options 03, 04 or 05 are installed in the counter, the effects of temperature perturbations and aging must still be considered, although the magnitude of the inaccuracies associated with each oscillator are greatly reduced.

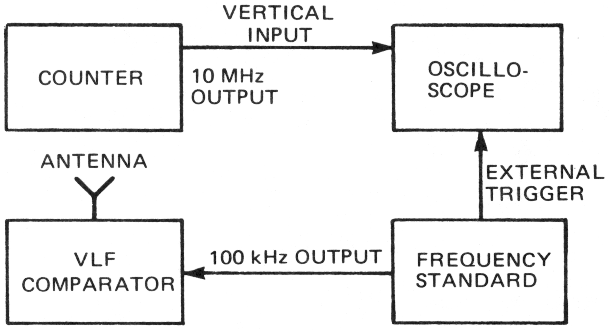
Full benefit of the oven stabilized oscillator characteristics can only be realized if the oscillator is running continuously (with counter always connected to a source of AC power). Under these conditions the perturbations in frequency will generally be in the positive direction for either an increase or decrease in temperature from + 25° C. The aging characteristic is also generally in the positive direction.

How frequently the oscillator is adjusted is determined by the level of accuracy required. To adjust the oscillator to an inaccuracy of less than 1×10^{-9} parts, relative to a standard, use this procedure. The test is illustrated in figure -5.

Observe the drift of the oscilloscope pattern. The fractional frequency offset is computed from:

$$\frac{T_{\text{drift of zero crossing}}}{T_{\text{observation time of drift}}} = \frac{\Delta f}{f}$$

If the pattern drifts, at a rate of .01 microsecond every 10 seconds, the frequency is in error by 1 part in 10^9.



OVEN OSCILLATOR A114

Figure 03/04/05-5. Time Base Calibration.

All frequency checks and adjustments should be made only after the oscillator has been connected to its power source for 24 hours. If the oscillator has been disconnected from its power source for more than 24 hours it may require 72 hours of continuous operation to achieve the specified frequency aging rate.

To measure oscillator frequency:

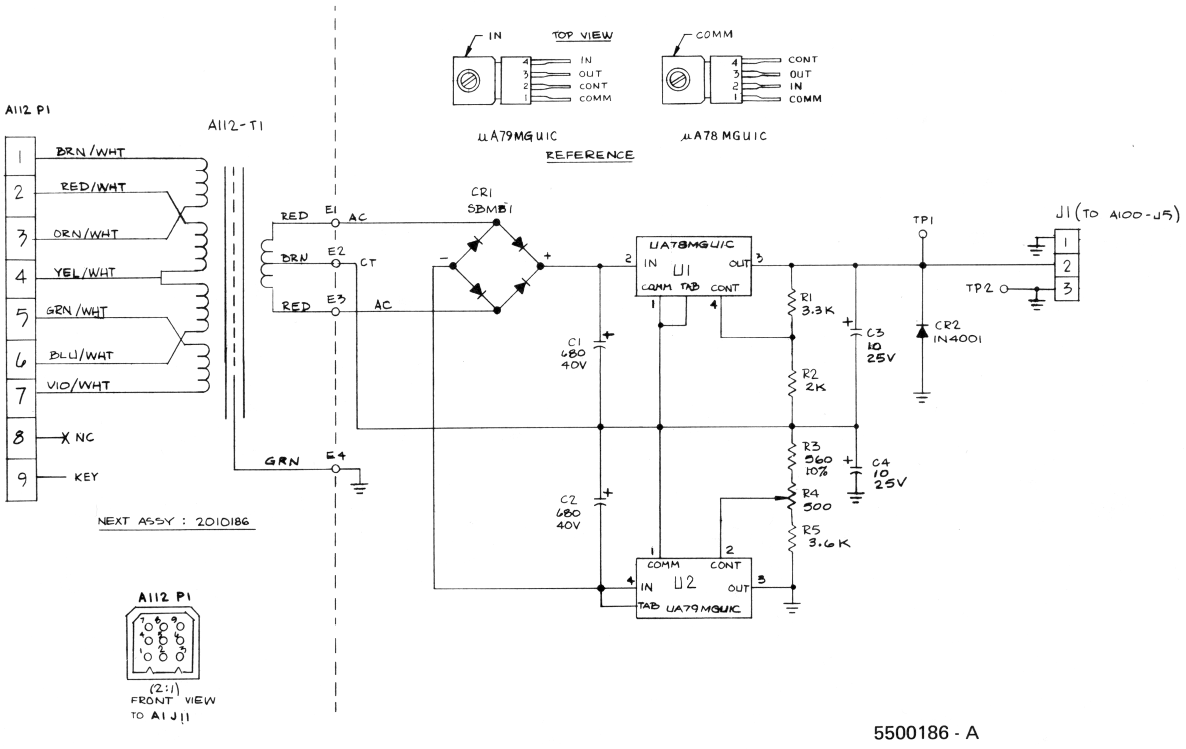
1. Connect the counter's internal oscillator output signal from the 10 MHz IN/OUT connector (on the rear panel of the counter) to the vertical input of the oscilloscope.
2. Trigger oscilloscope externally with the frequency standard. The VLF Comparator is used to determine the absolute frequency of the standard.
3. Set oscilloscope sweep rate to 0.1 μ sec/cm and expand X10; this results in a sweep rate of .01 μ sec/cm.
4. Adjust oscilloscope vertical controls for maximum gain.
5. Determine the frequency difference (see page 6-24).
6. Horizontal drift of oscilloscope display in μ sec/sec, is a measure of the difference between the frequency standard and the counter oscillator frequency. If the difference is excessive for the desired counter application, vary the TIME BASE ADJUST control on the rear panel of the counter until the pattern stops drifting.

NOTE

For highest accuracy, the counter should be operated for 72 hours prior to adjustment.

OPTION 03/04/05 - TIME BASE OSCILLATOR PCB ASSYs 2020186 - A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A112	OSCILLATOR POWER SUPPLY	2020186	1	EIP	
C1	Elec, 680 uF, 40V	2200021	2	307INF681T040B	80031
C2	C1				
C3	Tant, 10 uF, 25V	2300029	2	DF106M25S	NEC
C4	C3				
CR1	Bridge Rectifier	2700019	1	SBMB1	14099
CR2	Rectifier	2704001	1	IN4001	
R1	Met Ox, 3.3K, 2%	4130332	1	C$/2%/3.3K	24546
R2	Met Ox, 2K, 2%	4130202	1	C$/2%/2K	24646
R3	Met Ox, 560, 2%	4130561	1	C4/2%/560	24546
R4	Variable, Cer, 500, 10%	4250014	1	72XR500	73138
R5	Met Ox, 3.6K, 2%	4130362	1	C4/2%/3.6K	24546
U1	Positive Voltage Regulator	3040780	1	uA78MGUIC	07263
U2	Negative Voltage Regulator	3040790	1	uA79MGUIC	07263



IN
TOP VIEW
4 IN
3 OUT
2 CONT
1 COMM
µA79MGU1C
COMM
4 CONT
3 OUT
2 IN
1 COMM
µA78MGU1C
REFERENCE
A112 P1
A112-T1
1 BRN/WHT
2 RED/WHT
3 ORN/WHT
4 YEL/WHT
5 GRN/WHT
6 BLU/WHT
7 VIO/WHT
8 NC
9 KEY
NEXT ASSY : 2010186
RED E1 AC
BRN E2 CT
RED E3 AC
GRN E4
CR1 SBMB1
C1 680 40V
C2 680 40V
UA78MGU1C
IN U1 OUT
COMM TAB CONT
UA79MGU1C
COMM CONT
IN U2 OUT
TAB
R1 3.3K
R2 2K
R3 560 10%
R4 500
R5 3.6K
C3 10 25V
C4 10 25V
TP1
TP2
CR2 IN4001
J1 (TO A100-J5)
A112 P1
(2:1)
FRONT VIEW
TO A1 J11
5500186 - A

Figure 03/04/05-6. Time Base Option Schematic

OPTION 06
EXTENDED FREQUENCY CAPABILITY

The frequency range extension option is available on the 548A counter. This option, when used with the model 590 Frequency Extension Cable kit and one of the optional remote sensors, enables the counter to count signals above 26.5 GHz. The option consists of:

- Band 4 Converter Module, A204
- Band 4 Software
- Coax Cable, Front panel to A204 J1 - P/N 2040232
- Coax Cable, Front panel to A204 J2 - P/N 2040231

SPECIFICATIONS

BAND	FREQUENCY RANGE	SENSITIVITY (TYPICAL)	MAX. INPUT	REMOTE SENSOR MODEL
41	26.5-40 GHz	-25 dBm typ. -20 dBm min.	+5 dBm	91
42	40-60 GHz	-25 dBm	+5 dBm	92
43	60-90 GHz	-25 dBm	+5 dBm	93
44	90-110 GHz	-25 dBm	+5 dBm	94

OPERATION

To operate the counter in the 26.5 - 40 range, connect the short cable (supplied with the frequency extension kit) from the lower output jack on the front panel, to the Band 3 input. Connect the long cable from the upper outjack to the remote sensor.

PRESS:	BAND	BAND annunciator blinks
PRESS:	4	BAND 4 annunciator blinks
PRESS:	1	BAND 4 annunciator lights stays on

The counter is now in the proper mode for operation.

NOTE: Before connecting the remote sensor to the frequency source, verify that the power level is within the limits specified for the sensor. When you connect the sensor the counter will automatically display the reading.

THEORY OF OPERATION – HARDWARE

When measuring a signal frequency greater than 26.5 GHz the 548A using the Option 06 Frequency Extension with a model 590 kit and a 91 remote sensor, down converts the input to approximately 1.0 GHz. This signal is then fed to the Band 3 input, where a second conversion produces a 125 MHz IF.

A multiplier chain increases the VCO output frequency to the 5.28-6 GHz range, which is referenced to the time base. See Figure 06-1. This signal provides the local oscillator (LO) power, which is transmitted to the remote sensor, an external harmonic mixer. When the input frequency and harmonics of the LO, (generated in the mixer) combine, a first IF is generated in the range of 1.00-1.35 GHz.

A diplexer separates the LO and IF signals received from the harmonic mixer. The level of the IF is then increased to a minimum of -25 dBm via the IF amplifier, then supplied to the Band 3 converter input.

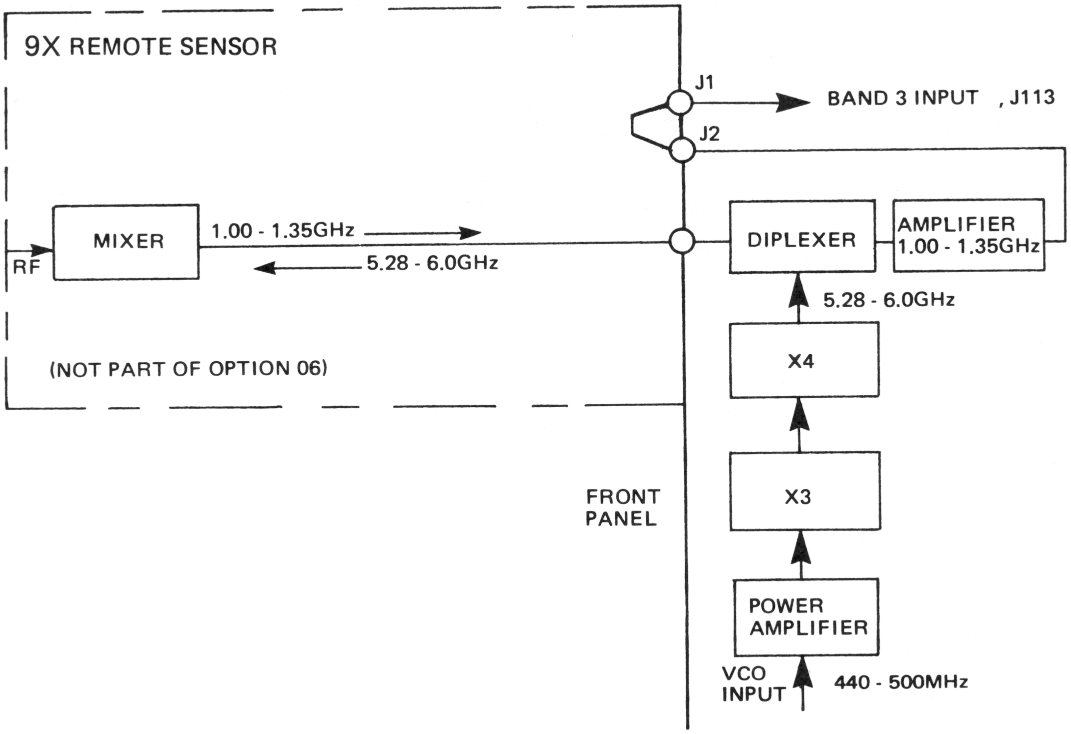

9X REMOTE SENSOR
J1
BAND 3 INPUT ,J113
J2
MIXER
RF
1.00 - 1.35GHz
5.28 - 6.0GHz
DIPLEXER
AMPLIFIER 1.00 - 1.35GHz
5.28 - 6.0GHz
X4
(NOT PART OF OPTION 06)
FRONT PANEL
X3
POWER AMPLIFIER
VCO INPUT
440 - 500MHz

Figure 06-1. Frequency Extension Block Diagram

THEORY OF OPERATION – SOFTWARE

Band 4 acquires a signal by using a double conversion process. The microprocessor has control over the YIG filter and the VCO, thus making it possible to compute the approximate RF input signal, and down-convert the IF signal so it can be counted.

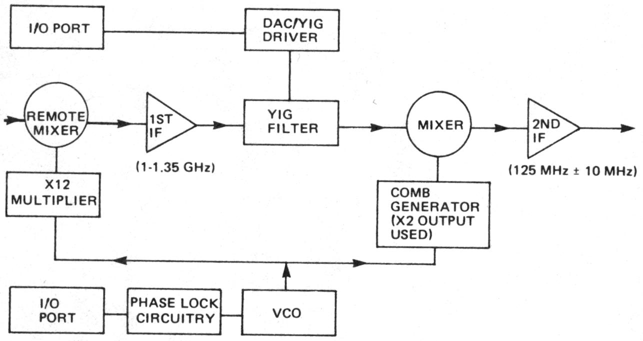

I/O PORT
DAC/YIG DRIVER
REMOTE MIXER
1ST IF
YIG FILTER
MIXER
2ND IF
(1-1.35 GHz)
(125 MHz ± 10 MHz)
X12 MULTIPLIER
COMB GENERATOR (X2 OUTPUT USED)
I/O PORT
PHASE LOCK CIRCUITRY
VCO

Figure 06-2. Down-conversion of Band 4 Signal

The following equations characterize this process.

$$\text{RF INPUT} = 12\text{ N } F_{VCO} \pm 1\text{st IF}$$

$$1\text{st IF} = 2\ F_{VCO} + 2\text{nd IF}$$

therefore:

$$\text{RF INPUT} = \underbrace{F_{VCO}}_{\text{Controlled by Processor}}\ \overbrace{(12N \pm 2)}^{\text{calculated}}\ \overbrace{\pm 2\text{nd IF}}^{\text{IF counted}}$$

Sign depends on hi/low side mixing to produce 1st IF.

Where N = the harmonic number which is mixing with the RF to produce the first IF.

There are two main functions that the Band 4 program performs. It locks on to an incoming RF signal, and tracks an RF signal once it is locked.

The locking routine is called by the supervisor when any of the following conditions are met.

1. Selection of Band 4
2. Loss of IF threshold after being locked
3. Any reset condition

The tracking routine is used under the following two conditions.

1. After locking, the tracking routine is used to "fine tune" the locked signal.
2. When the RF signal is moving, the tracking routine is used to give a constant update of corrected parameters so that the YIG filter and VCO can stay locked onto the signal.

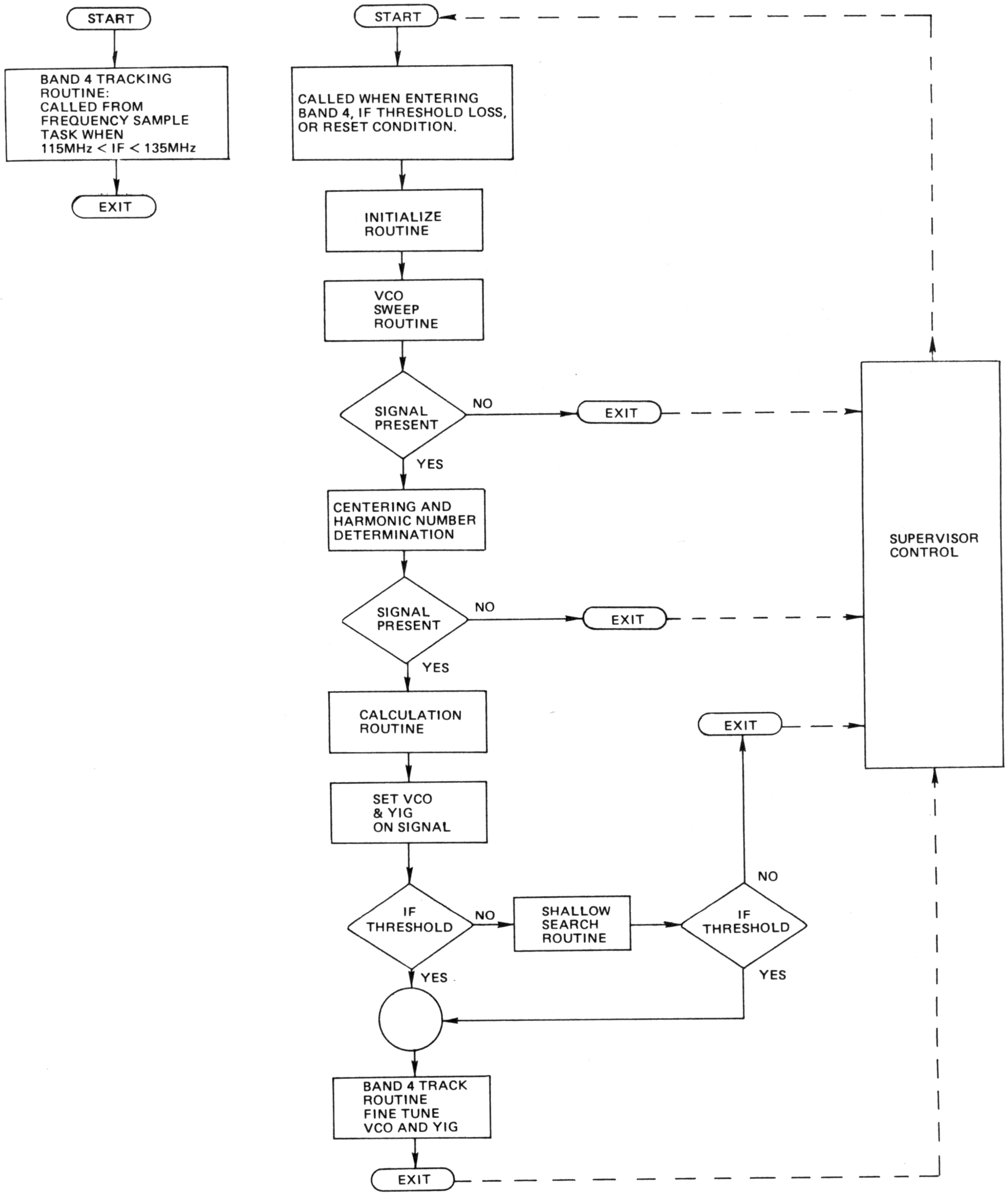

START
BAND 4 TRACKING ROUTINE: CALLED FROM FREQUENCY SAMPLE TASK WHEN 115MHz < IF < 135MHz
EXIT
START
CALLED WHEN ENTERING BAND 4, IF THRESHOLD LOSS, OR RESET CONDITION.
INITIALIZE ROUTINE
VCO SWEEP ROUTINE
SIGNAL PRESENT
NO
EXIT
YES
CENTERING AND HARMONIC NUMBER DETERMINATION
SIGNAL PRESENT
NO
EXIT
YES
SUPERVISOR CONTROL
CALCULATION ROUTINE
EXIT
SET VCO & YIG ON SIGNAL
NO
IF THRESHOLD
NO
SHALLOW SEARCH ROUTINE
IF THRESHOLD
YES
YES
BAND 4 TRACK ROUTINE FINE TUNE VCO AND YIG
EXIT

Figure 06-3. Band 4 Program, Flow Diagram

The process by which the program locks onto an RF signal is defined in the next six sections. Refer to Figure 06-3.

INITIALIZATION – The working table (BANDTP) for band 4 is cleared and the appropriate table of constants, used by the program for the particular Band 4 that has been selected, are loaded from PROM in this area. BANDTP is an area in RAM that is 27 bytes long.

VCO SWEEP – This routine steps the VCO frequency by a step size stored in BANDTP. After each step, the VCO frequency is checked for three stop points.

1. Top VCO frequency limit (500 MHz)
2. Wraparound frequency
3. Lockout frequency

If the top VCO frequency has been reached and no signal has been found, the program will return to the supervisor. If the top frequency is reached, and a signal has been detected, then the VCO is set to its low limit and the bottom range is searched until the wraparound frequency is reached.

If the wraparound frequency has been reached (the frequency at which the last VCO frequency has produced the strongest IF frequency), then the program will stay at this frequency, and will perform the centering and harmonic number determination routines.

If a lockout frequency (a VCO frequency at which erroneous locking results) is detected, the VCO frequency will be incremented by:

13 * STEP SIZE = NEW VCO FREQUENCY

and the program will continue from this frequency.

After each VCO step the YIG filter is swept to see if a signal is detected by the power DAC attenuator. If a signal was detected, the YIG is swept back and forth, and the attenuation is increased until the signal is lost. At this point a new VCO frequency is stepped and the process of signal detection continues, thus leaving the power DAC at the last setting to detect the next highest signal.

CENTERING AND HARMONIC NUMBER DETERMINATION – This routine will determine the harmonic number of the VCO which is causing the mix product to be in the proper range. (Refer to Figure 06-4).

First we obtain the proper step size for the calculation of the harmonic number (N). After the VCO sweep routine is complete and the VCO frequency is set, the incoming signal is mixed with a harmonic of the VCO frequency to produce a signal in a predetermined passband region. This signal is stepped to the outer edge of the passband (± step depending on whether the signal is high or low side mixed) by the following process.

1. Increment the VCO
2. Power level the IF signal
3. Center on the signal
4. Test for band limits

These steps are repeated until the edge of the passband is reached.

Harmonic Number N	Input Frequency Ranges	
	High Side Mixing (MHz)	Low Side Mixing (MHz)
5	25,395 – 28,875	27,405 – 31,125
6	30,675 – 34,875	32,685 – 37,125
7	35,955 – 40,875	37,965 – 43,125
8	41,235 – 46,875	43,245 – 49,125
9	46,515 – 56,875	48,525 – 55,125
10	51,795 – 58,875	53,805 – 61,125
11	57,075 – 64,875	59,085 – 67,125
12	62,355 – 70,875	64,365 – 73,125
13	67,635 – 76,875	69,645 – 79,125
14	72,915 – 82,875	74,925 – 85,125
15	78,195 – 88,875	80,205 – 91,125
16	83,475 – 94,875	85,485 – 97,125
17	88,755 – 100,875	90,765 – 103,125
18	94,035 – 106,875	96,045 – 109,125
19	99,135 – 112,875	101,325 – 115,125

Figure 06-4. Harmonic Mixing Ranges

Next the VCO is stepped back into the passband and a new centering takes place. This second center frequency is stored for later calculation of the harmonic number. Next the signal is stepped to the edge of the passband position it had just left, and it is centered. This center frequency is now compared to the first edge of the passband center frequency, and must be within 8 MHz. If it is not within 8 MHz it will be assumed that the signal is moving, and the Band 4 program is exited.

The IF frequency step size, caused by the VCO frequency step, is used to determine the harmonic number by the following equation.

$$\frac{\Delta \text{ IF FREQ. DUE TO VCO STEP}}{\text{HARMONIC SPACING}} = \text{HARMONIC \#(N)}$$

Where harmonic spacing = VCO step size X 12

CALCULATION ROUTINE – The calculation routine is used to find the approximate RF frequency Fin in the following manner.

1. Compute $F' = 12\,N * F_{VCO}$
2. Center the YIG filter on the first IF
3. Convert the binary YIG frequency to BCD
4. Compute $F_{IN} = F' \pm F_{YIG}$ (where F_{YIG} gives the approximate value for the first IF).
5. Compute a corrected VCO frequency using the equation:

$$F_{VCO} = (F_{IN} \pm 125) / (12N \pm 2)$$

Then tune the VCO with the corrected frequency and center the first IF frequency in the yig passband.

SHALLOW SEARCH – This routine tests for a signal in the IF passband. If a signal is present, the routine is exited. If a signal is not present, the routine will search an RF range of ±60 MHz (in steps of 200 kHz), for the signal, and continues if a signal is found. If a signal is not found, the Band 4 program returns control to the supervisor.

BAND 4 TRACKING – The tracking routine centers the second IF in the following range.

$$115 \text{ MHz} < \text{2nd IF SIGNAL} < 135 \text{ MHz}$$

This routine is called from outside of the Band 4 program to track a signal. A test is first made to determine if an IF threshold is present. If IF threshold is present it continues, if not the program returns to the supervisor to start the locking process from the beginning.

This routine reads the second IF frequency and computes the new VCO frequency so that the second IF is in the range given above. A new YIG frequency is calculated and the VCO and YIG are "tuned" to produce a new IF. A new FLO (frequency added to the second IF to produce the displayed frequency), is calculated. The equation for this process is:

$$F_{LO} = F_{VCO} (12 N \pm 2)$$

The YIG frequency is: NEW F_{YIG} = 2 (NEW VCO) + 125 MHz.

PERFORMANCE TESTS

The Band 4 converter module is not field repairable. When a malfunction is suspected, its operation can be checked from the front panel as follows:

IF AMPLIFIER	Apply a -50 dBm signal to the diplexer port (upper output jack) from 1.0 to 1.35 GHz. Output should be -3 dBm ±3 dB as checked on a spectrum analyzer connected to the IF output (lower jack).
LO SIGNAL	Connect a spectrum analyzer to the diplexer port (upper output jack). Using the following formula, set the VCO frequency between 440 and 500 MHz. The spectrum analyzer should show the 12th harmonic of the VCO frequency (5.28-6 GHz). The spectrum analyzer signal should be +8 dBm minimum, and free of breakup and spurious signals to -30 dBc.

To convert from the desired VCO frequency to the PIA program number:

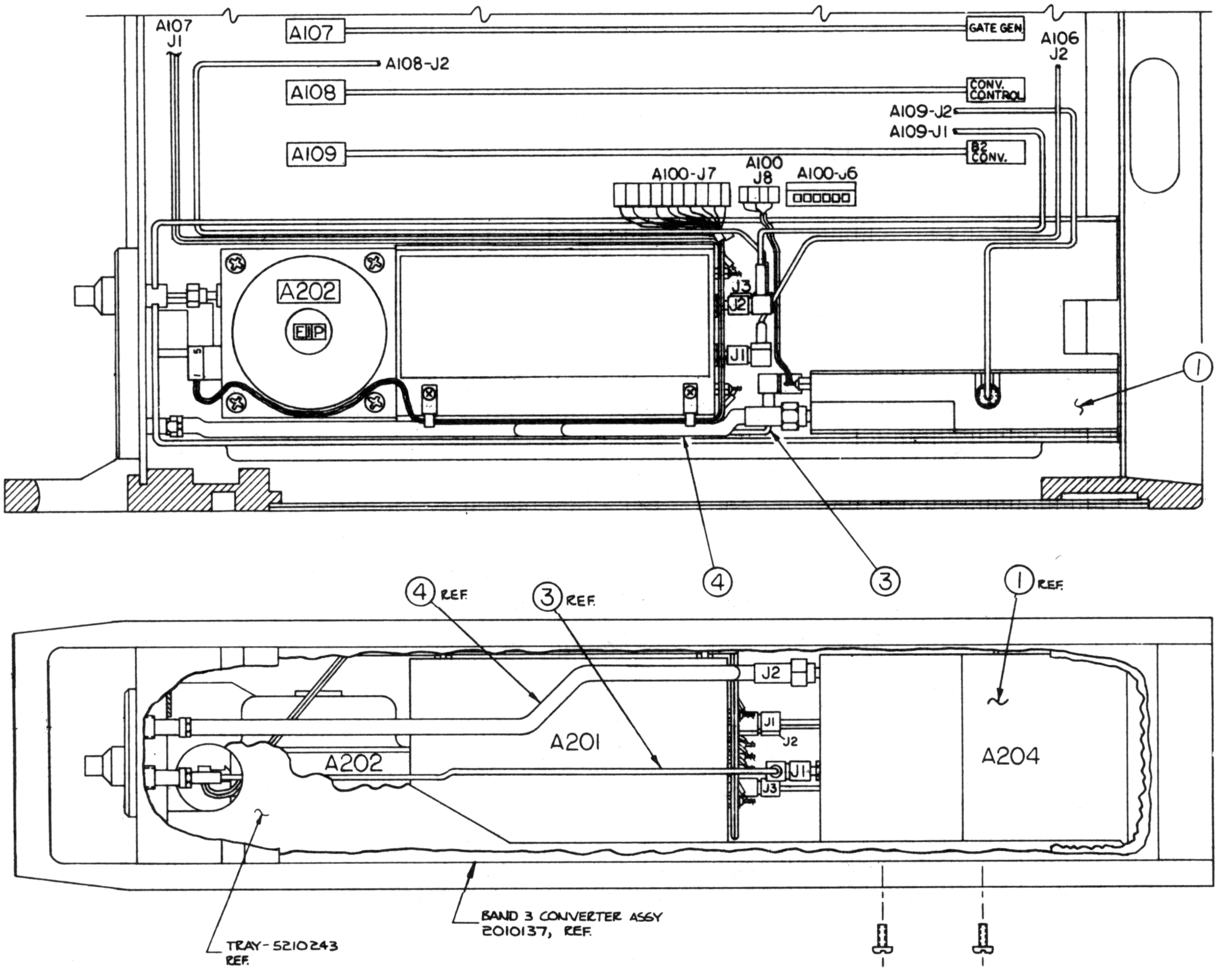
EXAMPLE (440.75 MHz)

1. Round the desired frequency to a multiple of 50 KHz (The resolution of the VCO frequency is 50 KHz).
2. Multiply the desired frequency (in MHz) by 5 . . . . 440.75 X 5 = 2203.75
3. If the result contains no fractional part, go to step 8.
4. Multiply only the fractional part by 16 .75 x 16 = 12
5. Add the result to the most significant digit from step 2 . . . . MSD of 2203.75 = 2 – 2 + 12 = 14
6. Convert the result to hexadecimal . . . . $14_{10} = E_{16}$
7. Replace the MSD from step 2 with the result from step 6 and drop the fractional part . . . . 2203.75 → E203
8. The two most significant digits are programmed to address 9822, and the two least significant digits are programmed to address 9820.

To remove a defective converter:

1. Remove the line cord and both the top and bottom cover of the counter.
2. Remove the two screws holding the converter in place from the bottom.
3. Remove coaxial cables and unplug DC harness.
4. Lift the converter out of the counter.

To replace, proceed in the reverse order. See Figure 06-5 for location of the converter in the counter.


A107 J1
A107
A108-J2
A108
A109
GATE GEN.
A106 J2
CONV. CONTROL
A109-J2
A109-J1
B2 CONV.
A100-J7
A100 J8
A100-J6
A202
J3
J2
J1
①
④
③
④ REF.
③ REF.
① REF.
J2
J1
J2
J1
J3
A201
A202
A204
BAND 3 CONVERTER ASSY 2010137, REF.
TRAY-5210243 REF.

① Band 4 Converter – 2010229

③ Cable (FP to A204J1) – 2040232-01

④ Cable (FP to A204J2) – 2040231-01

Figure 06-5. Location of Installed Band 4 Converter (A204)

OPTION 07
REMOTE PROGRAMMING/BCD OUTPUT

This option makes it possible to use a conventional printer or other readout device, and remotely program the functions that are normally done on the front panel of the counter.

SPECIFICATIONS

BCD OUTPUT

FORMAT	11 digits plus sign in parallel
"0" STATE	0.4 Volts at 4mA
"1" STATE	2.7 Volts at -400μA
NEGATIVE REF.	Ground
POSITIVE REF.	+5 Volts at 2K Ω Source Impedance
PRINT COMMAND	20 μs wide TTL Low level logic signal
INHIBIT INPUT	2 to 50 Volts High level logic signal

REMOTE PROGRAMMING

INPUT LOADING	1 Low power Shottky TTL load plus 10K pull up to +5 Volts
FUNCTIONS	All front panel controls except: Power ON/OFF, Sample rate, Clear Display, and test functions greater than 01.
OUTPUT LEVEL	Refer to "0" State and "1" State for BCD.

OPERATION

BCD OUTPUT

This binary-coded decimal (BCD) output (plus sign information) represents any numerical data that would normally be displayed by the eleven digits on the front panel of the counter. When the information being displayed represents the frequency alone the minus sign refers to the frequency. When the information being displayed represents frequency and power the minus sign refers to the power.

A 20 microsecond print command is provided to indicate when the data is valid. An inhibit command is provided that will prevent the data from being altered.

BCD OUTPUT PIN CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	10^1 A	16	10^8 B	31	10^3 D	46	10^0 C
2	10^1 B	17	10^9 A	32	10^4 C	47	10^0 D
3	10^2 A	18	10^9 B	33	10^4 D	48	Print Command
4	10^2 B	19	10^{10} A	34	10^5 C	49	Minus Sign
5	10^3 A	20	10^{10} B	35	10^5 D	50	Ground
6	10^3 B	21	10^0 A	36	10^6 C		
7	10^4 A	22	Inhibit	37	10^6 D		
8	10^4 B	23	10^0 B	38	10^7 C		
9	10^5 A	24	−Ref.	39	10^7 D		
10	10^5 B	25	+Ref.	40	10^8 C		
11	10^6 A	26	10^1 C	41	10^8 D		
12	10^6 B	27	10^1 D	42	10^9 C		
13	10^7 A	28	10^2 C	43	10^9 D		
14	10^7 B	29	10^2 D	44	10^{10} C		
15	10^8 A	30	10^3 C	45	10^{10} D		

NOTE

The 10^0 bit is the least significant digit, and corresponds to the 1 Hz output.

A, B, C, and D are the 1, 2, 4, and 8 bits of each binary coded decimal output digit.

REMOTE PROGRAMMING

All front panel functions can be remotely programmed except the Power on/off, Sample Rate, Clear Display, and test functions greater than 01. All the inputs are activated by a ground contact closure, or a "0" level TTL signal (0 = true). The input load is equal to one low power shottky TTL load, plus a 10 KΩ pullup to +5 volts.

CONTROL LINE FUNCTIONS

REMOTE ENABLE – A low level on this line transfers counter control from the front panel keyboard to the rear panel remote programming connector.

INPUT DATA – A low level on this line initiates a data read cycle to read the function/program data contained on the 22 data input lines. If this line is held low the counter will continuously poll the input data.

DATA ACCEPTED – This signal is output from the counter to the controller. The line goes high when data is being read by the counter, and goes low upon completion of a data read cycle.

PROGRAM DATA – A low level on this line indicates that the 22 data lines will be interpreted as program data. A high level on this line indicates that these lines will be interpreted as function data.

DATA LINE FUNCTIONS

RESET COUNTER – A low level on this line will reset the counter and initiate a new search for a valid signal.

UPDATE READING – A low level on this line will cause the counter to take a new reading, update the front panel display, and update the BCD output.

BAND SELECT (3 lines) – These lines select the band, or Test 01, in accordance with the following:

C	B	A	BAND
0	0	0	Test 01
0	0	1	Band 1
0	1	0	Band 2
0	1	1	Band 3
1	0	0	Band 4.1*
1	0	1	Band 4.2*
1	1	0	Band 4.3*
1	1	1	Band 4.4*

---

*In counters that do not have Option 6, the C bit does not apply.

RESOLUTION (4 lines) – These lines program the remote resolution. A four digit BCD number (0 through 9) will indicate the number of digits that are blanked.

DAC SELECT (4 lines) – These lines select the most significant digit of the DAC option (01), when it is installed in the counter. A hexadecimal number (1 to B) will select digit 1 to 11 as the MSD of the 3 digits output to the DAC. Any other digit disables the DAC option.

HOLD MODE – A low level on this line will place the counter in the hold mode (data not updated until the counter is reset).

FAST CYCLE – A low level on this line will place the counter in the fast cycle mode (no display time).

POWER METER – A low level on this line will enable the power meter on counters with Option 02.

VIEW FUNCTION LINES (5 lines) – A low level on one of these lines will cause the counter to display the indicated function on the front panel and the BCD output. If more than one line is enabled at a time, the counter will display the first one found in the following order.

1. DAC Select
2. Frequency Limit Low
3. Frequency Limit High
4. Frequenty Offset
5. Power Offset

PROGRAM LINE FUNCTIONS

PROGRAM SELECT (2 lines) – These two lines select one of four functions to be programmed by the program data in accordance with the following.

SELECT b	BIT a	FUNCTION PROGRAMMED
0	0	Frequency limit low
0	1	Frequency limit high
1	0	Frequency Offset
1	1	Power Offset

MINUS SIGN – When this line is low the four digits of programming data are interpreted as a negative number.

EXPONENT (3 lines) – These three lines are interpreted as a BCD number (0 to 7). This number is the power of 10 that is to be multiplied, times the four digits of data (data X 10^x). This multiplier is used for all frequency input data, and is ignored for the power input data.

DIGIT 1 TO DIGIT IV (4 lines each) – These are four BCD digits that represent the input data. Digit 1 is the MSD and Digit IV is the LSD. For power input, a decimal point is located between Digit II and Digit III, and Digit IV is not used.

DATA ENTRY

Preceeding any data entry sequence, the counter must be placed in the remote mode (remote enable line low). Once in remote mode, the input data line is brought low to initiate a data read sequence. The data read is normally function data. When the program data line is brought low, the data read will be interpreted as program data. The data accept line will go high to indicate that the data has been latched in, and will remain high while the counter processes this data.

Figure 07-1 shows the data entry timing sequence. The input data line debounce time (1) is typically 16 to 18 ms. Data is latched into the counter 48 μs before the data accept line goes high (2). As soon as the data accept line goes high, all data (except remote enable) can be removed. The data accept line stays high while the counter processes the input data. This process is data dependent, and can take from 1 to 140 ms (3). To prevent the counter from setting the poll mode, the input data line must go high within 100 μs after the data accept line goes low (4). If poll mode is set, the next data read cycle will occur between 0 and 100 ms after the high to low transition of the data accept line. After this first data read cycle, all subsequent data read cycles will occur at 100 ms intervals.

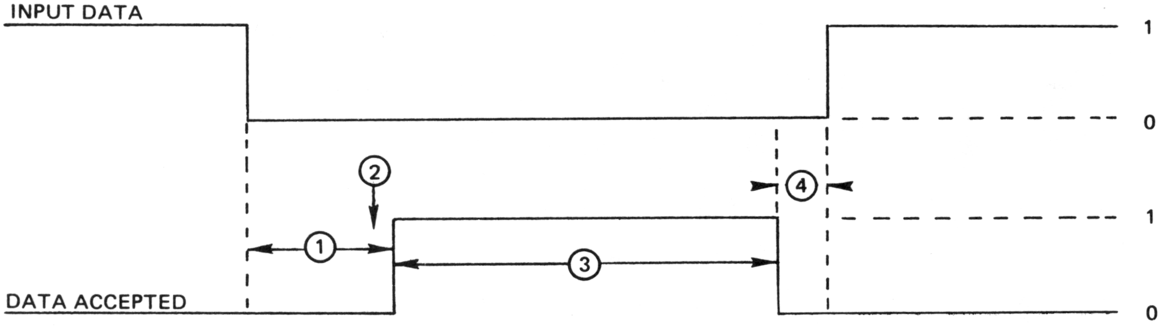


Figure 07-1. Data Entry Timing

DATA ENTRY EXAMPLE

The following example remotely programs the counter to be in Band 3 with 1 kHz resolution, and a −160 MHz frequency offset.

1. Put counter in remote mode by bringing the remote enable line low.
2. Set the program data to be entered by bringing the program data line low.
   a. Set digit 1=1
      Set digit 2=6
      Set digit 3=0
      Set digit 4=0
   b. Set the exponent =5 (1600 x 10^5)
   c. Set program select A=0, B=1 (frequency offset)
   d. Set minus sign low (negative offset)
3. Enter program data by bringing the input data line low until the data accept line goes high.
4. Set the remote function data.
   a. Return all lines high except the remote enable line.
   b. Set the resolution A and B lines low (resolution 3).
   c. Set the Band select C line low (Band 3).

   NOTE: Counters that do not have Option 06 (Band 4) will set Band 3, even with the select line C high.
5. Enter function data by bringing the input data line low until the data accept line goes high.

REMOTE PROGRAMMING PIN CONNECTIONS

PIN	FUNCTION DATA	PROGRAM DATA
1-5	BCD Data (Do not use these pins)	
6-12	Ground	
13	DAC Select A	Digit II A
14	DAC Select B	Digit II B
15	DAC Select C	Digit II C
16	DAC Select D	Digit II D
17	Resolution A	Digit I A
18	Resolution B	Digit I B
19	Resolution C	Digit I C
20	Resolution D	Digit I D
21-24	No connection	
25	Program Data) Control Lines	Program Data) Control Lines
26	Remote Enable)	Remote Enable)
27	Input Data)	Input Data)
28	Data Accepted)	Data Accepted)
29	View Power Offset	Digit IV A
30	View Frequency Offset	Digit IV B
31	View Frequency Limit High	Digit IV C
32	View Frequency Limit Low	Digit IV D
33	View DAC Select	Digit III A
34	Power Meter Enable	Digit III B
35	Fast Cycle Mode	Digit III C
36	Hold Mode	Digit III D
37	Ground	Ground
38-44	No connection	
45	Band Select A	Exponent A
46	Band Select B	Exponent B
47	Band Select C	Exponent C
48	(No function)	Minus Sign
49	Update Reading	Program Select A
50	Reset Counter	Program Select B

THEORY OF OPERATION

The BCD/REMOTE programming board takes data from the display and formats it as parallel data output for the rear panel. It also receives counter control and programming information from the 26 line input on the rear panel to provide for remote control of the counter.

BCD THEORY OF OPERATION

During each update cycle, the counter checks for the existence of the BCD/RMT board. If the board exists, the program checks the state of the inhibit input. If the inhibit input is true (+2 to +50V on the input), the program jumps past the BCD output but the counter continues to update the display. If the input is low, the program scans through each of the 11 digits (LSB to MSB). Each digit is checked, and any non-numerical digit is replaced by a zero. The resulting BCD digit is then sent to U2 through 4 bits of port B of the PIA (U14). After each digit is made available to U2, 4 clock pulses (BCD Clock) are sent to U2 (through U7) to shift all the data in the shift registers to the right by 4 bits (1 digit). At the end of these data shift pulses, a BCD load pulse enters the new data into U2. When the last digit (MSB) is entered into U2, the sign bit is simultaneously entered into U1. After all the data has been entered into the shift register, the program sends out a 20 microsecond print command.

REMOTE PROGRAMMING THEORY OF OPERATION

When the remote enable line is high, none of the other remote programming lines can effect the counter. When the remote enable line is brought low, the counter changes from local to remote operating conditions and switches control for the counter from the front panel keyboard to the rear panel remote programming connector. When in the remote mode, the counter waits for an input from the INPUT DATA request line. When the input data line is brought low, the data direction control line is sent low to put U9 in the low impedance buffer mode. The RMT LOAD line is then toggled to load all remote input data into the input registers (U8-U12). The counter then changes the data accepted output from a low to a high to indicate that the data has been read. The 8 bits of data into U14 (from U8 and U10), are read by the microprocessor. Groups of 4 clock pulses are then sent out (on the RMT CLOCK line), to shift the input data into U10 where the data is read by the microprocessor through U14. When all the data has been read, the data direction control line is returned to a high level, and the data accept line is returned to low, indicating the data has been accepted by the counter.

When the INPUT DATA line is held low, the counter sets a flag and returns to read the input data at approximately 100 millisecond intervals. This continues until the INPUT DATA line is returned to high, at which time the counter returns to the condition where it is waiting for a high to low transition on the INPUT DATA line.

When the remote enable line is returned to the high state (local mode), the counter exercises a clear display function and then returns to the (previous) local mode condition.

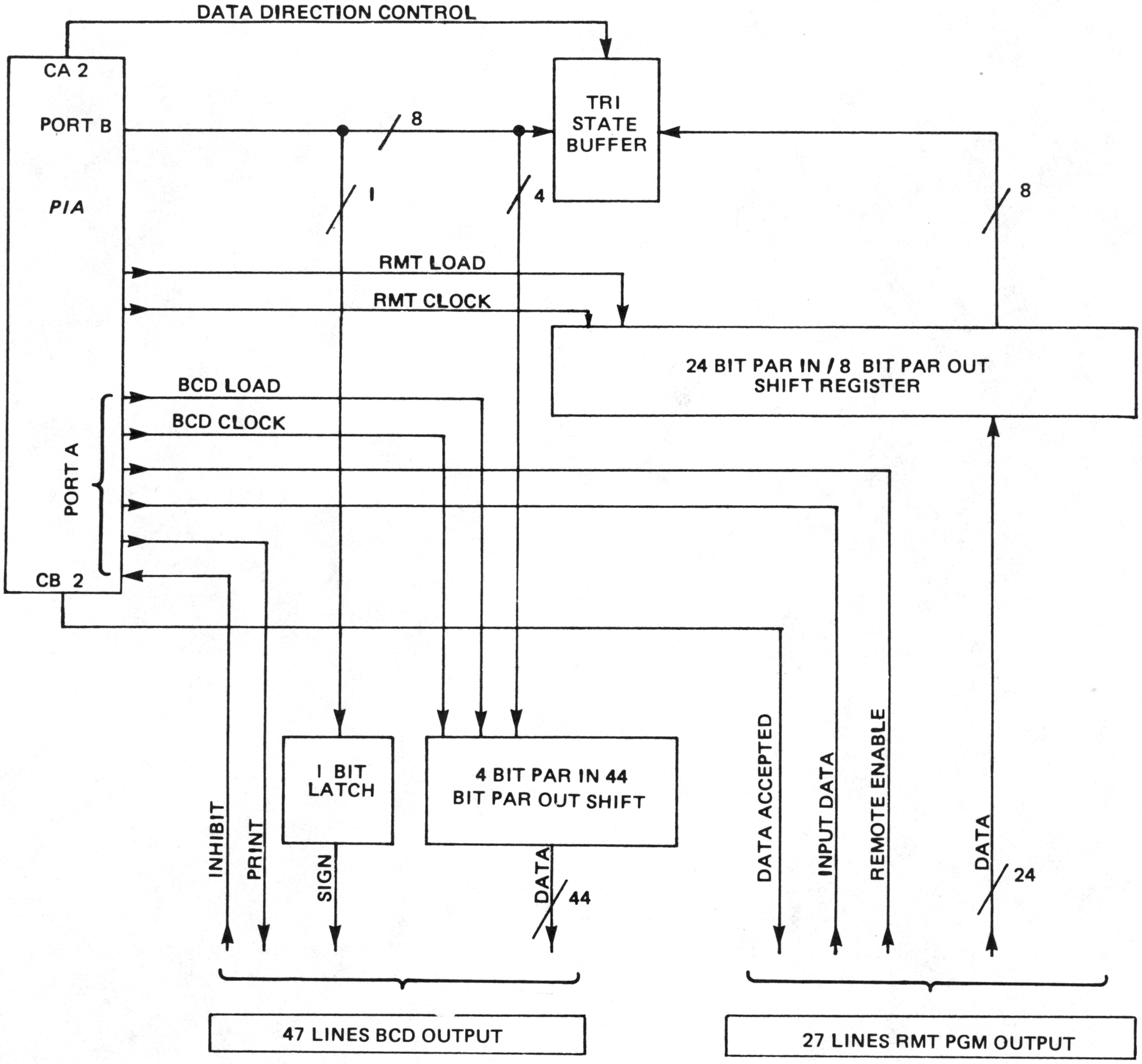
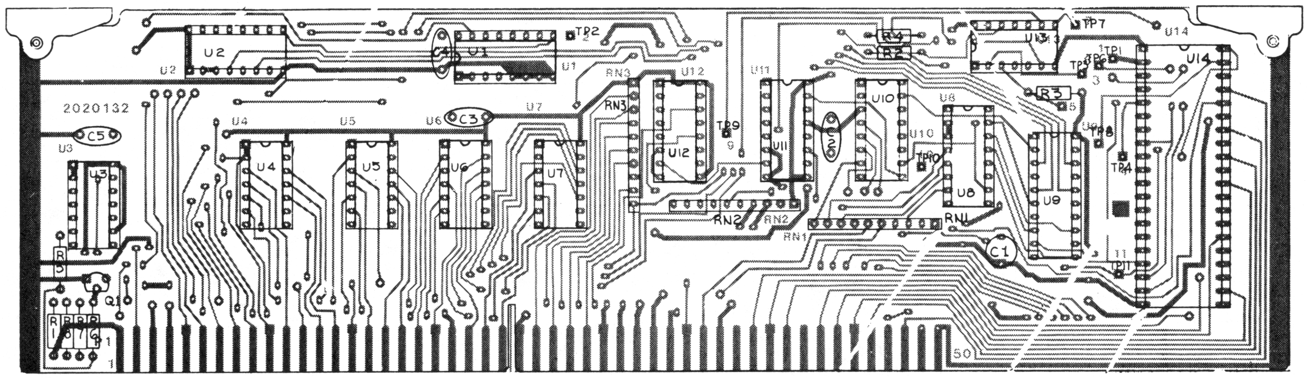

DATA DIRECTION CONTROL
CA 2
PORT B
PIA
PORT A
CB 2
TRI STATE BUFFER
8
1
4
8
RMT LOAD
RMT CLOCK
24 BIT PAR IN / 8 BIT PAR OUT SHIFT REGISTER
BCD LOAD
BCD CLOCK
1 BIT LATCH
4 BIT PAR IN 44 BIT PAR OUT SHIFT
INHIBIT
PRINT
SIGN
DATA
44
DATA ACCEPTED
INPUT DATA
REMOTE ENABLE
DATA
24
47 LINES BCD OUTPUT
27 LINES RMT PGM OUTPUT

Figure 07-2. Remote Programming/BCD Output Simplified Block Diagram

OPTION 07 - REMOTE PROGRAMMING / BCD OUTPUT

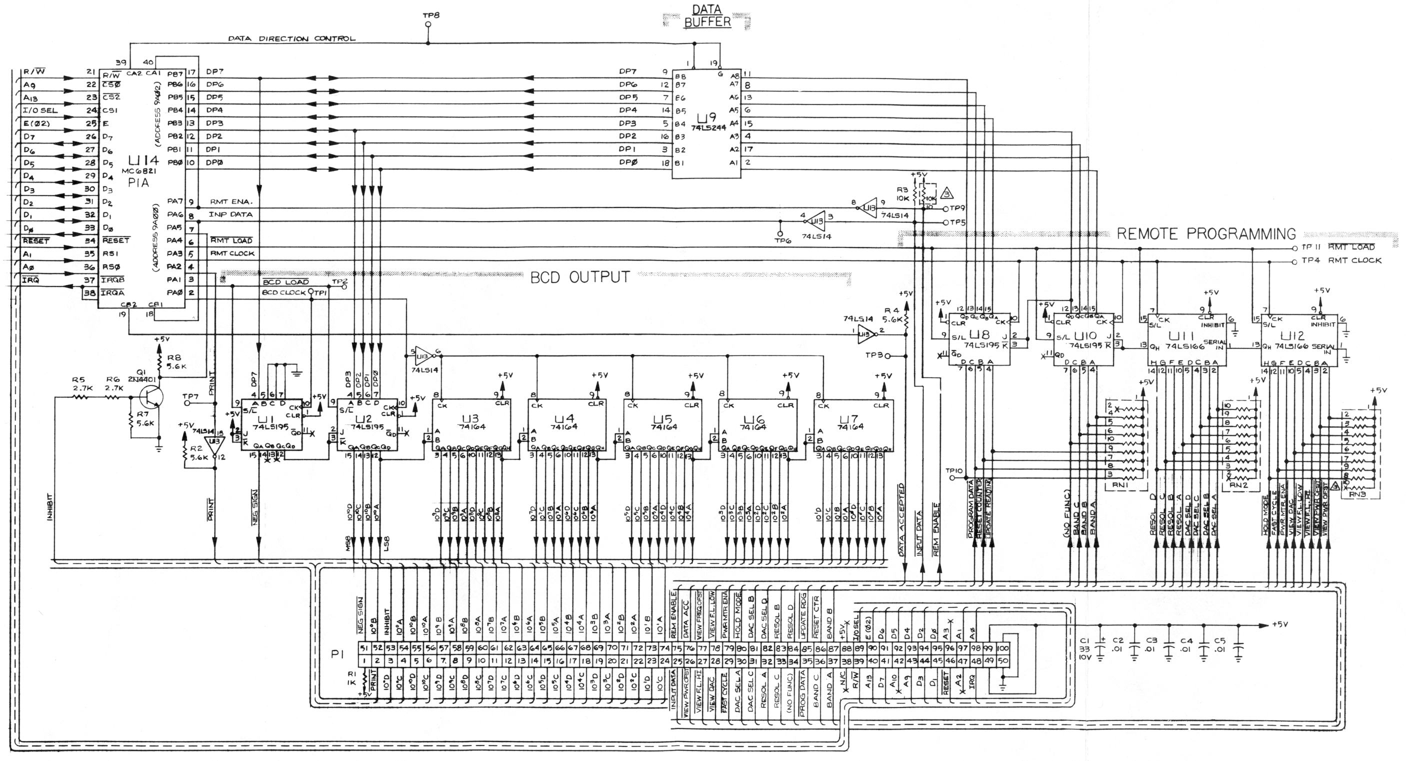
2010231 - A

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
07	REMOTE PROGRAMMING / BCD , PCB	2020132		EIP	
-1	Bail Mount Kit	5000195	1	3475-1	76381
-2	Cable, Flat Ribbon (to A100 J2, J3)	2040176-01	2		
-3	PCB Assy, A102 A	2020132	1	EIP	
C1	Tant, 33uF, 10%, 10V	2300015	1	TAG-20-33/10-50	14433
C2 thru C5	Cer, .01uF, 20%, 100V	2150003	4	TAG-S10	56289
Q1	Transistor, NPN	4704401	1	2N4401	04713
R1	Comp, 1 K, 5 %, ¼ W	4010102	1	RC07GF102J	81349
R2	Comp, 5.6K, 5%, ¼ W	4010562	4	RC07GF562J	81349
R3	Comp, 10K, 5%, 1/8 W	4010103	1	RC07GF103J	81349
R4	R2				
R5	Comp, 2.7K, 5%, ¼ W	4010272	2	RC07GF272J	81349
R6	R5				
R7	R2				
R8	R2				
RN1 thru RN3	Network, 10 pin , 10K, ± 2%, 1.25W	4170003	3	4310R-101-103	32997
TP1 thru TP11	.040 Dia. Conn. Pin	2620032	11	460-2970-02-03	71279
U1	4 bit Shift Register	3084195	4	SN74LS195AN	01295
U2	U1				
U3 thru U7	8 Bit Parallel OUT Register	3074164	5	DM74164	01295
U8	U1				
U9	Line Driver/Octal Buffer Inverter	3084244	1	SN74LS244N	01295
U10	U1				
U11	8 bit Shift Register	3084166	2	SN74LS166N	01295
U12	U11				
U13	Hex Inverter/Schmitt Trig.	3087414	1	SM74LS14N	01295
U14	P.I.A.	3086821	1	MC6821	04713
A105					
U16	PROM Set	2060002-05	1		


U2
C4
U1
TP2
U2
U1
RN3
U12
U11
R4
R2
U13
TP7
U14
TP1
TP6
TP5
U14
2020132
U4
U5
U6
C3
U7
RN3
R3
C5
U3
TP9
U12
U11
U10
U10
U8
TP10
U9
TP8
TP4
U4
U5
U6
U7
RN2
RN2
RN1
RN1
U8
U9
C1
TP11
Q1
R5
R1
R8
R7
R6
1
50

2020132 - B

Figure 07-3. Remote Programming / BCD Output, Component Locator


DATA BUFFER
DATA DIRECTION CONTROL
TP8
U14
MC6821
PIA
(ADDRESS 9A02)
(ADDRESS 9A00)
R/W
A0
A13
I/O SEL
E(Ø2)
D7
D6
D5
D4
D3
D2
D1
D0
RESET
A1
A0
IRQ
DP7
DP6
DP5
DP4
DP3
DP2
DP1
DP0
RMT ENA.
INP DATA
RMT LOAD
RMT CLOCK
BCD LOAD
BCD CLOCK
TP1
BCD OUTPUT
U9
74LS244
REMOTE PROGRAMMING
TP11 RMT LOAD
TP4 RMT CLOCK
R3 10K
TP9
TP5
TP6
74LS14
R4 5.6K
TP3
U8 74LS195
U10 74LS195
U11 74LS166
U12 74LS166
RN1
RN2
RN3
TP10
Q1 2N4401
R5 2.7K
R6 2.7K
R7 5.6K
R8 5.6K
R2 5.6K
TP7
U1 74LS195
U2 74LS195
U3 74164
U4 74164
U5 74164
U6 74164
U7 74164
U13
INHIBIT
PRINT
NEG SIGN
MSB
LSB
DATA ACCEPTED
INPUT DATA
REM ENABLE
P1
R1 1K
+5V
C1 33 10V
C2 .01
C3 .01
C4 .01
C5 .01

I.C. NO.	TYPE	PIN NO.	
		GND	+5V
U1,U2,U8,U10	74LS195	8	16
U3,4,5,6,7	74164	7	14
U11,U12	74LS166	8	16
U9	74LS244	10	20
U13	74LS14	7	14
U14	MC6821	1	20

⚠3 RESISTOR AT TP9 PART OF RN3 PIN 10.

5500132 - B

Figure 07-4. Remote Programming/BCD Output Schematic Diagram

OPTION 08

GENERAL PURPOSE INTERFACE BUS

Option 08 makes 545A/548A microwave counters fully compatible with the General Purpose Interface Bus (GPIB). With this option the counter can respond to remote control instructions and can output measurement results via the IEEE 488-1978 Bus interface. At the simplest level the counter can output data to other devices such as the HP 5150A Thermal Printer. In more sophisticated systems a calculator or other system controller can remotely program the counter, trigger measurements, and read results. Of course, a calculator or computer adds other benefits to a GPIB based measurement system. The calculator can manipulate data to compute the mean and standard deviation, check for linearity, and compare results to limits, or perform many other functions.

GPIB FUNCTIONS IMPLEMENTED

The GPIB interface function subsets implemented are:

SH1	complete capability
AH1	complete capability
T5	basic talker, serial poll, Talk Only mode, unaddress if MLA
L3	basic listener, Listen Only mode, unaddress if MTA
SR1	complete capability
RL1	complete capability
DC1	complete capability
DT1	complete capability

NOTE

When DEVICE CLEAR or SELECTED DEVICE CLEAR GPIB bus command is received, the counter will revert to the power on state. When DEVICE TRIGGER GPIB bus command is received, the counter will initiate a new frequency reading cycle. The converter will not be reset.

SETTING ADDRESS SWITCH

The counter employs a decimal address switch located inside the unit. This is set for decimal address 19 at the factory. To verify the switch setting without removing the top of the counter, simply initiate test 10; enter 9C04 and read the address on the display. A description of test 10 can be found on page 6-7. After reading the address, terminate the test by pushing the clear display key.

The address switch is also used to put the counter in the Talk Only (to) or Listen Only (lo) mode. To put the counter in the Listen Only mode simply set the address switch to any number 41 or higher.

The counter can be put in four different modes of operation in the Talk Only mode. The following is a list of the address settings for entering these modes.

ADDRESS	MODE OF OPERATION
32	Continuous output determined by SAMPLE RATE control. Exponent in scientific format.
33	Continuous output - fast active. SAMPLE RATE control inactive. Exponent in scientific format.
34	Continuous output determined by SAMPLE RATE control. Exponent in zero output format.
35	Continuous output - fast active. SAMPLE RATE control inactive. Exponent in zero output format.

NOTE

In the Talk Only or the Listen Only mode, the address of the counter is always automatically set to decimal 0.

DEVICE DEPENDENT DATA INPUT

It takes a specific amount of time for the counter to process the input data (error checking, formatting, changing the mode of operation, etc.). To prevent the data rate of the bus from slowing down while the counter is doing input data processing, the data is accepted as soon as it is available on the bus, and it is temporarily stored in memory. The size of the storage memory is 100 characters.

The users of the GPIB option need to be aware that there is a difference between accepting data and complying with it. If the counter is asked to output a reading before it has finished processing the input data, the output will be in error if the operator makes the assumption that the counter is in the mode that was just programmed. To prevent this, sufficient programmed delays must be provided, or use must be made of the counter's Service Request status byte. See Service Request (SR) command description.

GPIB INSTRUCTION FORMAT

<OP CODE> <NUMBER> <TERMINATOR>

OPERATION CODE or OP CODE can take any of the following formats:

<LETTER> <LETTER> or <LETTER> <DIGIT>

Example: FH (Frequency limit high) or B3 (band 3)

The NUMBER portion of the statement can take the form of any of the following:

<SIGN> <DIGIT STRING>

Example: –2457

<SIGN> <DIGIT STRING> • <DIGIT STRING>

Example: –3.483

NOTE: Spaces within the <OP CODE> and <NUMBER> portions of the instructions are always ignored.

The TERMINATOR allows the operator to choose the scale of an input number as well as implement special functions.

TERMINATOR = G/M/K/H/D/P/C

G, M, K, H, represent GHz, MHz, kHz and Hz respectively
D = dB, P = clear data, (equivalent to "clear data" key on keyboard)
C = clear display (equivalent to "clear display" key on keyboard)

FORMAL DEFINITION OF INSTRUCTIONS

<OP CODE> <NUMBER> <TERMINATOR>

<OP CODE> :: = <LETTER> <LETTER> | <LETTER> <DIGIT>

<NUMBER> :: = <SIGN> <DIGIT STRING> |
<SIGN> <DIGIT STRING> • <DIGIT STRING> |
NULL

<TERMINATOR> :: = G | M | K | H | D | P | C | NULL

<SIGN> :: = + | − | NULL

<DIGIT STRING> :: <DIGIT> <DIGIT> <DIGIT> - - - - - - -

<LETTER> :: = A | B | C | D | E | F | G | H | I | J | K | L | M | N |
O | P | Q | R | S | T | U | V | W | X | Y | Z

<DIGIT> :: = 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 0

PROGRAM CODE SET

Codes underlined indicate start-up conditions. These conditions are set by the device clear or selected device clear, or power on.

DISPLAY

DA – Display Active: Output Frequency Reading to Front Panel and Bus
DP – Display Passive: Output Frequency Reading to Bus only
DN – Display Normal

BAND

B1 – Band 1: 10Hz - 100MHz
B2 – Band 2: 10MHz - 1GHz
B3 – Band 3: 1GHz - 18GHz (Model 545A) / 26.5GHz (Model 548A)
B4 – Band 4: (Model 548A / Option 06)

RESOLUTION

R0 – Resolution 0 = 1Hz
R1 – Resolution 1 = 10Hz
R2 – Resolution 2 = 100Hz
R3 – Resolution 3 = 1KHz
R4 – Resolution 4 = 10KHz
R5 – Resolution 5 = 100KHz
R6 – Resolution 6 = 1MHz
R7 – Resolution 7 = 10MHz
R8 – Resolution 8 = 100MHz
R9 – Resolution 9 = 1GHz

MEASUREMENT FUNCTIONS

FA – Fast Active (Ignore sample rate Pot)
FP – Fast Passive (Terminates FA)
RS – Reset Basic Counter and Converter. Take a new reading after reset.
HA – Hold Active
HP – Hold Passive

DATA MANIPULATION FUNCTIONS

FO – Frequency Offset. Take a new reading after data entry if counter not in hold.
PO – Power Offset. Take a new reading after data entry if counter not in hold.
*OA – Offset Active:
—Add Frequency Offset to Frequency Reading
—Add Power Offset to Power Reading if Power Meter Function is active
OP – Offset Passive (Terminates OA)
ML – Multiplier. Multiplies frequency readings by an integer number.

---

*In Start-up Condition, although OA is Active, "0" (zero) Frequency and Power Offsets are programmed.

POWER METER

PA — Power Meter Option Active. Initiate a new gate.
PP — Power Meter Option Passive (Terminates PA)

*MEASUREMENT PARAMETERS

FH — Frequency Limit High. Basic counter and converter will be reset after data entry.
FL — Frequency Limit Low. Basic counter and converter will be reset after data entry.

SELF-TEST FUNCTIONS

TA — Test Active.
TP — Test Passive. (clear test function)

DATA FORMAT

EZ — Exponent Zero
ES — Exponent Scientific

DATA OUTPUT

BR — Output both frequency and power readings
FR — Output frequency readings only
PR — Output power readings only

SERVICE REQUEST

SR — Service request enable

DAC OPTION

DC — Select DAC option

*Measurement parameters: Standard Software
Limits of 950MHz (LOW) and 18.5GHz (HIGH) (27GHz for Model 548A) are featured in each counter at turn on.

DESCRIPTION OF AVAILABLE COMMANDS

DISPLAY

DA — Display Active - Outputs readings to both front panel and GPIB bus

DP — Display Passive - Outputs readings to GPIB bus only. It will decrease the cycle time of the counter.

DN — Display Normal - Resets display only; used for clearing error messages on the display. Cannot be used after verifying preprogrammed data such as Frequency Offsets or Frequency Limits. This OPCODE affects only the display.

BAND

B1 — Selects Band 1

B2 — Selects Band 2

B3 — Selects Band 3

B4 — Selects Band 4. Requires an additional digit input to designate individual remote sensors.

Example: B41 = remote sensor 1 which covers range of 26.5 to 40GHz.

RESOLUTION

R0 thru
R9 — Resolution 0 thru 9 - Picks the front panel resolution from 1Hz to 1GHz. Also chooses gate time which is related to resolution: 1Hz = 1 Sec, 10Hz = 100 Sec. 100Hz = 10 msec. 1kHz to 1GHz = 1 msec.

MEASUREMENT FUNCTIONS

FA — Fast Active - Causes the counter to go into the fast cycle mode of operation. In this mode, the front panel sample rate/hold control is inactive and the fastest sample rate is attained. The counter will not go into the Fast Active mode of operation until Hold Active is disabled.

FP — Fast Passive - Terminates FA.

RS — Reset Basic Counter and Converter - Re-acquires input signal and takes a new reading. Has the same function as manual reset button.

HA — Hold Active - The counter stops taking readings and the last frequency and power readings are displayed and held. The counter can be directed to take one reading when it is in this mode by sending Device Trigger or Selected Device Trigger GPIB bus command to the counter. It will also update the reading if the RS mnemonic is received.

HP — Hold Passive - Terminates HA.

DATA MANIPULATION FUNCTIONS

FO — Frequency Offset - Enables entry of frequency offsets. (1 Hz resolution available.) A new gate will be initiated after data entry if counter is not in HOLD.

PO — Power Offset - Enables entry of power offsets. Take a new reading after data entry if counter is not in HOLD.

OA — Offset Active - Add frequency offset to frequency readings. Add power offset to power readings if power meter function is active.

OP — Offset Passive - Does not add frequency and power offset to readings.

ML — Multiplier - Enables entry of a 2-digit frequency readings multiplier. The multiplier must be an integer between 00 and 99. The results are to 1kHz resolution. A new reading will be initiated after the data entry if the counter is not in HOLD. If the results of the multiplications are larger than, or equal to 999.999999999GHz, the counter will output 999.999999999GHz to the bus if asked to output readings.

POWER METER

PA — Power Active - Enables power meter option.

PP — Power Passive - Terminates power meter option.

MEASUREMENT PARAMETERS

FH — Frequency Limit High - Enables entry of frequency limit high (10 MHz resolution available). The basic counter and converter will be reset after the data entry.

FL — Frequency Limit Low - Enables entry of frequency limit low (10 MHz resolution available). The basic counter and conveter will be reset after the data entry.

SELF-TEST FUNCTIONS

TA — Test Active - Enables the counter to perform the selected test function by entering the mnemonic TA followed by two digits. When Test 05, 08, 09, or 10 is active and the counter is being asked to output data, the data that is displayed on the front panel is the data being output.

The output data format is as follows:

XXXXXXXXXXXXCRLF

X = alpha-numeric
CR = carriage return
LF = line feed

For detailed descriptions of tests 01 through 09 and test 11, see the section on Keyboard Controlled Circuit Tests.

Test 10 operates in the following manner:

1. To activate Test 10 input TA10.
2. To read the data stored in a specific memory location, input the address of the memory location in a four digit hexadecimal number. Enable the counter to talk and then read data from the counter.
3. To alter the data stored in a certain memory location:

   If 2. has been performed - input the desired data for that memory location.

   If 2. has not been performed - input the memory address, followed by a two digit hexadecimal number.

TP — Test Passive - Terminates test function.

DATA FORMAT

EZ — Exponent Zero - output format.

ES — Exponent Scientific - output format.

DATA OUTPUT

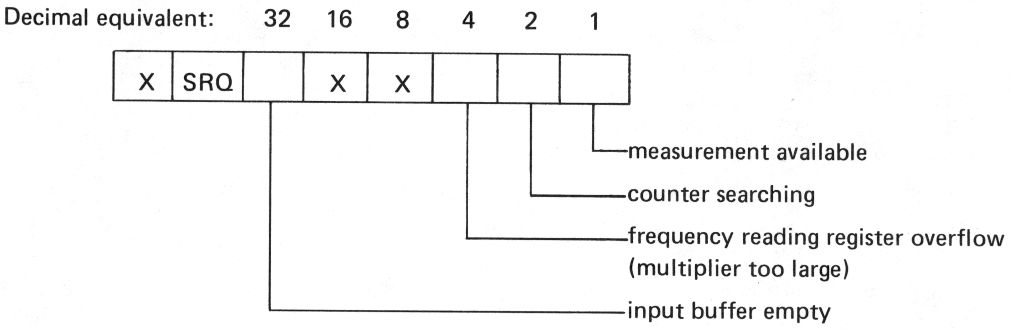
BR — Output both frequency and power readings. (See section on output data format.)

FR — Output frequency readings only. (See section on output data format.)

PR — Output power readings only. (See section on output data format.)

SERVICE REQUEST

SR — Service Request Enable - Enables the counter to send Service Request to the bus when a certain event has taken place in the counter. To enable the function, input SR followed by two decimal digits. The two digits are the decimal equivalent of the content of the eight bit status register. More than one bit of the status register can be set.


Decimal equivalent:
32
16
8
4
2
1
X
SRQ
X
X
measurement available
counter searching
frequency reading register overflow (multiplier too large)
input buffer empty

To disable the Service Request function, input SR00.

NOTE

Even when the Service Request function is disabled, the Service Request status byte will still be continuously altered to reflect the internal states of the counter.

EXAMPLE: To enable service request on measurement available and input buffer empty, send SR33.

DAC OPTION

DC — DAC Option - Enables the DAC option to convert three consecutive digits to an analog voltage, available on the rear panel. The output will reflect the display, and zeros are substituted for any non-numeric characters that appear. The output will be updated after every display update.

DC00 — turns DAC option off
DC01 — selects 1 Hz digit
thru
DC12 — selects 100 GHz, 10GHz and 1 GHz digits.

DATA OUTPUT FORMAT

The 545A/548A transmit the following string of characters to output a measurement.

Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Format																		
EZ (Exponent Zero)	b̸	±	D	D	D	D	D	D	D	D	D	D	D	D	E	0	CR	LF
ES (Exponent SCI)*	±	D	D	D	D	D	D	D	D	D	D	D	D	D	E	D	CR	LF
Power**	b̸	b̸	b̸	b̸	b̸	b̸	b̸	b̸	b̸	b̸	±	D	D	D	.	D	CR	LF

Freq. + Power

- FREQ in EZ mode: b̸ ± D D D D D D D D D D D D E 0 , b̸b̸b̸b̸b̸b̸b̸b̸b̸b̸ ± D D D . D CR LF
- FREQ in ES mode: ± D D D D D D D D D D D D D E D , b̸b̸b̸b̸b̸b̸b̸b̸b̸b̸ ± D D D . D CR LF

When the counter is in Test 05, 08, 09, or 10, the output will reflect the data on the display. The format is as follows:

XXXXXXXXXXXXCRLF.

b̸ = Blank
D = Digit
X = Alpha-numeric
CR = Carriage Return
LF = Line Feed

*in Exponent Scientific one digit represents the position of the decimal point. Exponent digit can be either 0, 3, 6, or 9.

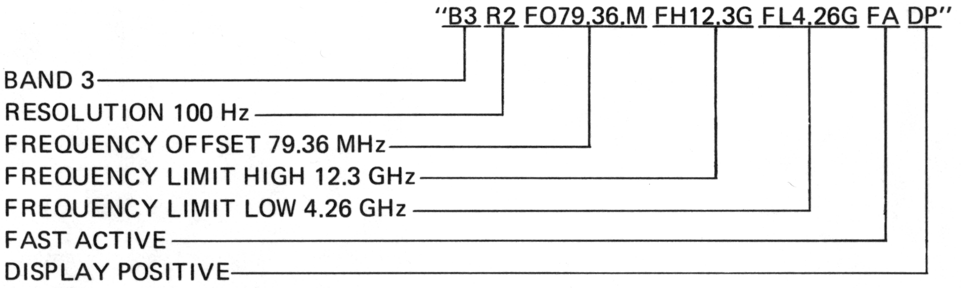
**The power information always have the decimal point fixed for 0.1dB resolution.

Under different output modes, the following counter outputs can be expected by a listener.

OUTPUT MODE	COUNTER OPERATING MODE	OUTPUT
BR	PA	FREQ + PWR
	PP	FREQ
	TA01	FREQ
FR	PA	FREQ
	PP	FREQ
	TA01	FREQ
PR	PA	PWR
	PP	–999.9
	TA01	–999.9
BR, FR or PR	TA 05, 08, 09, or 10	Data on front panel display

PROGRAM EXAMPLES

The examples given here assume an address setting of decimal 19 or ASCII talk address "S" and listen address "3" for the counter. By addressing the counter to listen and sending the following program string, it sets up the following measurement conditions.


"B3 R2 FO79.36.M FH12.3G FL4.26G FA DP"
BAND 3
RESOLUTION 100 Hz
FREQUENCY OFFSET 79.36 MHz
FREQUENCY LIMIT HIGH 12.3 GHz
FREQUENCY LIMIT LOW 4.26 GHz
FAST ACTIVE
DISPLAY POSITIVE

The following programs illustrate how controllers function with the counter. These programs cause the counter to make a series of frequency measurements. The calculators read the measurements into memory and print the results. The programs assume the counter Talk and Listen address is decimal "19."

```
HP 9825A    0:   dim A (10)
            1:   rem 7
            2:   wrt 719, "B3R2FO-4.55M"
            3:   wait 300
            4:   for 1 = 1 to 10
            5:   red 719, A (I)
            6:   prt A (I)
            7:   next I
            8:   end
HP 9845A   10:   output 719, "B3R2FO-4.55M '
           15:   wait 300
           20:   input 719, A
           30:   print "Frequency minus offset equals," A
           40:   Go to 20
TED 4051   10:   print @19: "B3R2FO-4.55M"
           20:   input @ 19: A
           30:   print "Frequency minus offset equals," A
           40:   Go to 20
```

The 9825A program will cause the counter to take a series of ten readings, print them on the 9825A paper tape and stop. Notice that an offset of 4.55 MHz is subtracted from each reading.

The program shown for the 9845A and TEK 4051 cause the counter to make a frequency measurement and print that measurement. To end the program, initiate a "STOP" command. This is accomplished on the 9845A with the key labeled "STOP." On the TEK 4051 use the key labeled "BREAK." To restart the program enter the RUN statement followed by the line number that is printed in the INTERRUPT message.

READING A MEASUREMENT

To read a measurement from the counter to a calculator, the counter must first be addressed to talk and the calculator to listen. The examples below indicate how a calculator may read a measurement from the counter.

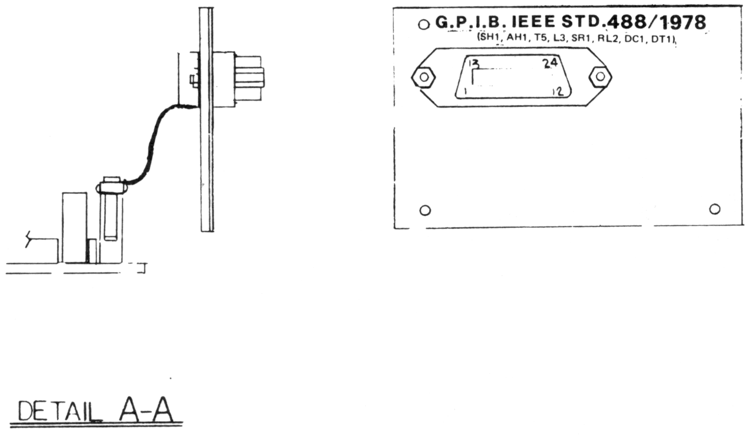
```
10 red 719, A    }                  10 input @ 19:A   }
                 }  HP 9825A                          }  TEK 4051
20 prt A         }                  20 print A        }

10 enter 719, A  }
                 }  HP 9845A
20 print A       }
```

The EIP counters can use two different modes. HA which takes one reading then waits for a reset command or a Device Trigger GPIB Bus Command. In this condition the counter is sent a reset or Device Trigger and (when addressed to talk) a new reading is output to the BUS. The counter will hold that particular reading on the display until another reset command or Device Trigger command is received. The other mode is HP or HOLD PASSIVE. In this mode data is read out in a normal BUS fashion. The display automatically updates corresponding to the sample rate chosen. In this condition successive readings can be output without generating a reset or Device Trigger command each time.

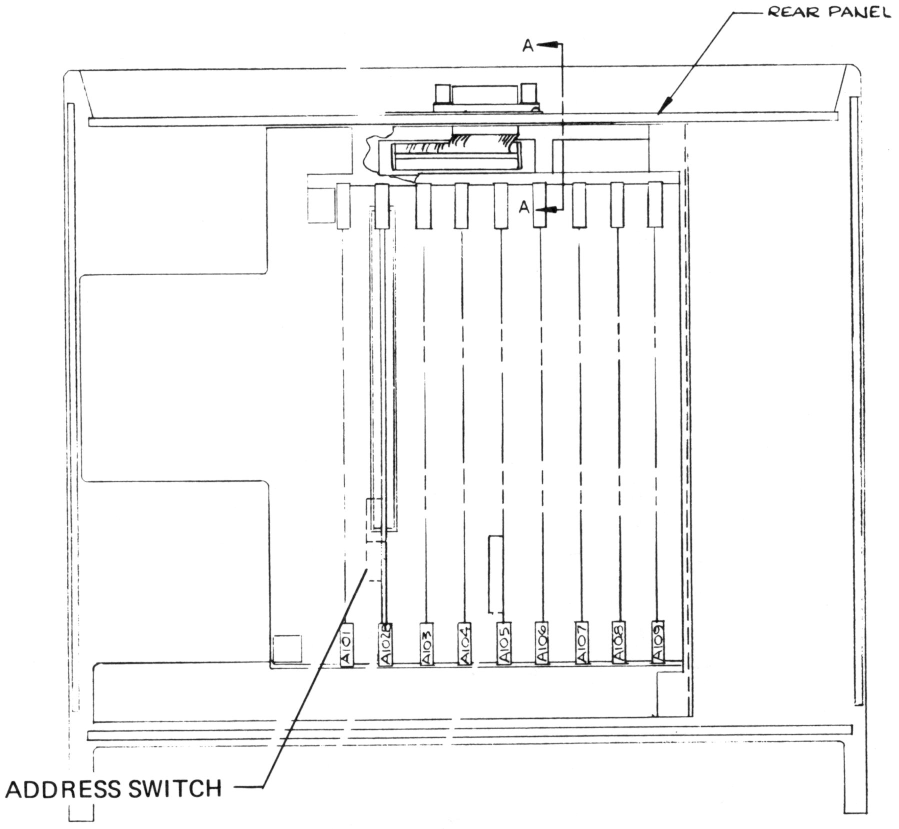
ADDRESS CHARACTERS		ADDRESS CODES					
Listen	Talk	binary					decimal
		5	4	3	2	1	*
SP	@	0	0	0	0	0	00
!	A	0	0	0	0	1	01
''	B	0	0	0	1	0	02
#	C	0	0	0	1	1	03
$	D	0	0	1	0	0	04
%	E	0	0	1	0	1	05
&	F	0	0	1	1	0	06
'	G	0	0	1	1	1	07
(	H	0	1	0	0	0	08
)	I	0	1	0	0	1	09
*	J	0	1	0	1	0	10
+	K	0	1	0	1	1	11
,	L	0	1	1	0	0	12
—	M	0	1	1	0	1	13
.	N	0	1	1	1	0	14
/	O	0	1	1	1	1	15
0	P	1	0	0	0	0	16
1	Q	1	0	0	0	1	17
2	R	1	0	0	1	0	18
3	S	1	0	0	1	1	19
4	T	1	0	1	0	0	20
5	U	1	0	1	0	1	21
6	V	1	0	1	1	0	22
7	W	1	0	1	1	1	23
8	X	1	1	0	0	0	24
9	Y	1	1	0	0	1	25
:	Z	1	1	0	1	0	26
;	[	1	1	0	1	1	27
<	/	1	1	1	0	0	28
=	]	1	1	1	0	1	29
>	^	1	1	1	1	0	30

* Decimal Talk/Listen Address is provided as a cross reference for those controllers which use decimal address.

Figure 08-1. Allowable Address Codes


G.P.I.B. IEEE STD.488/1978
(SH1, AH1, T5, L3, SR1, RL2, DC1, DT1)
13
24
1
12
DETAIL A-A

CONTACT	SIGNAL LINE	CONTACT	SIGNAL LINE
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI	17	REN
6	DAV	18	GND. (6)
7	NRFD	19	GND. (7)
8	NDAC	20	GND. (8)
9	IFC	21	GND. (9)
10	SRQ	22	GND. (10)
11	ATN	23	GND. (11)
12	SHIELD	24	GND. LOGIC

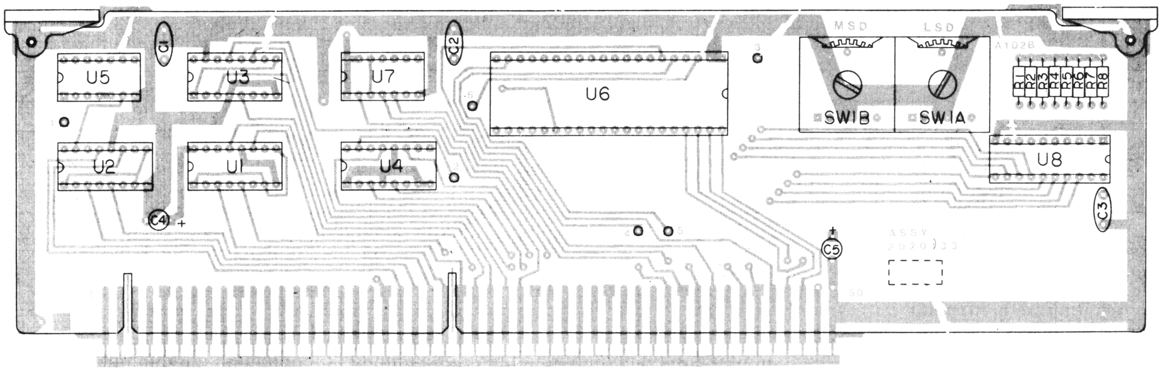

REAR PANEL
A
A
A101
A102
A103
A104
A105
A106
A107
A108
A109
ADDRESS SWITCH

SEE G.P.I.B MANUAL FOR ADDRESS SETTING INSTRUCTIONS.

Figure 08-2. **Location of GPIB in Counter**

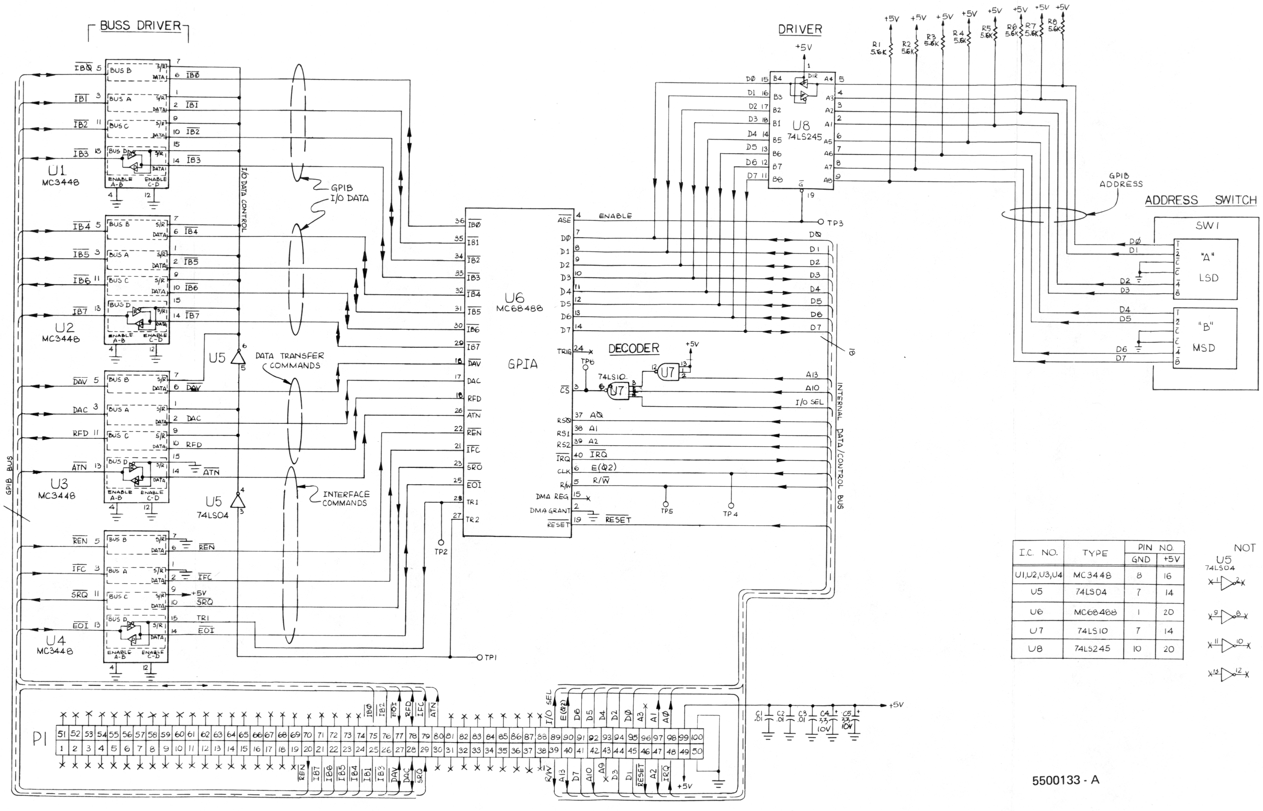
OPTION 08—GENERAL PURPOSE INTERFACE BUS

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
08	GPIB Option	2010232		EIP	
-1	PCB Assy, GPIB (A102B)	2020133	1	EIP	
C1	Cer, .01μF, %, V	2150003	3	TG - S10	56289
C2	C1				
C3	C1				
C4	Tant, 33μF, %, 10V	2300015	2	TAG20 - 33/10 - 50	14433
C5	C4				
R1 thru R8	Comp, 5.6K, 5%, W	4010562	8	RC07GF562J	81349
SW1A and SW1B	Thumbwheel Switch	4540004	2	1X2270 - 0000	
TP1 thru TP6	P.C. pin .040 diameter	2620032	6	460-2970-02-03	71279
U1 thru U4	Quad 3-state Bus Transciever	3053448	4	MC3448	04713
U5	Hex Inverter	3087404	1	74LS04	27014
U6	General Purpose Interface Adaptor	3058488	1	MC68488	04713
U7	Tri Input NAND Gate	3087410	1	74LS10	27014
U8	Oct Bus Transciever	3084245	1	74LS245	27014
	Cable, Flat Ribbon (Rear Panel to A100 J2)	2040177	1	EIP	
A105					
U16	PROM Set	2060002-02	1	EIP	


C1
C2
U5
U3
U7
U6
MSD
LSD
A102B
SW1B
SW1A
R1
R2
R3
R4
R5
R6
R7
R8
U2
U1
U4
U8
C3
C4
+
+
C5
ASSY
2020133
50

2020133 - B

Figure 08-3. GPIB Component Locator


BUSS DRIVER
U1
MC3448
U2
MC3448
U3
MC3448
U4
MC3448
U5
74LS04
GPIB I/O DATA
DATA TRANSFER COMMANDS
INTERFACE COMMANDS
I/O DATA CONTROL
GPIB BUS
U6
MC68488
GPIA
DECODER
74LS10
U7
DRIVER
U8
74LS245
GPIB ADDRESS
ADDRESS SWITCH
SW1
"A"
LSD
"B"
MSD
INTERNAL DATA/CONTROL BUS
TP1
TP2
TP3
TP4
TP5
TP6
P1
+5V
NOT USED

I.C. NO.	TYPE	PIN NO.	
		GND	+5V
U1,U2,U3,U4	MC3448	8	16
U5	74LS04	7	14
U6	MC68488	1	20
U7	74LS10	7	14
U8	74LS245	10	20

5500133 - A

Figure 08-4. GPIB Schematic

OPTION 09
REAR PANEL INPUT

Option 09 provides rear panel input for 545A/548A counters and counters equipped with option 06 in the following manner:

545A / 548A COUNTERS :

1. Reversing the converter assembly so that the Band 3 input connector protrudes through the hole in the rear panel that is identified as J113.

2. Reversing the Band 1 and Band 2 connectors to the holes marked J111 and J112 respectively on the rear panel.

Option 06 Equipped Counters:

1. Reversing the converter assembly so that the Band 3 input connector protrudes through the hole in the rear panel that is identified as J113. Reversing the Remote Sensor and Band 3 jumper connectors to the holes marked J114A (Rmt. Sensor) and J114B (Band 3 connector) respectively.

2. Reversing the Band 1 and Band 2 connectors to the holes marked J111 and J112 respectively on the rear panel.

NOTE: The specifications for the counter do not change when the input is from the rear panel.

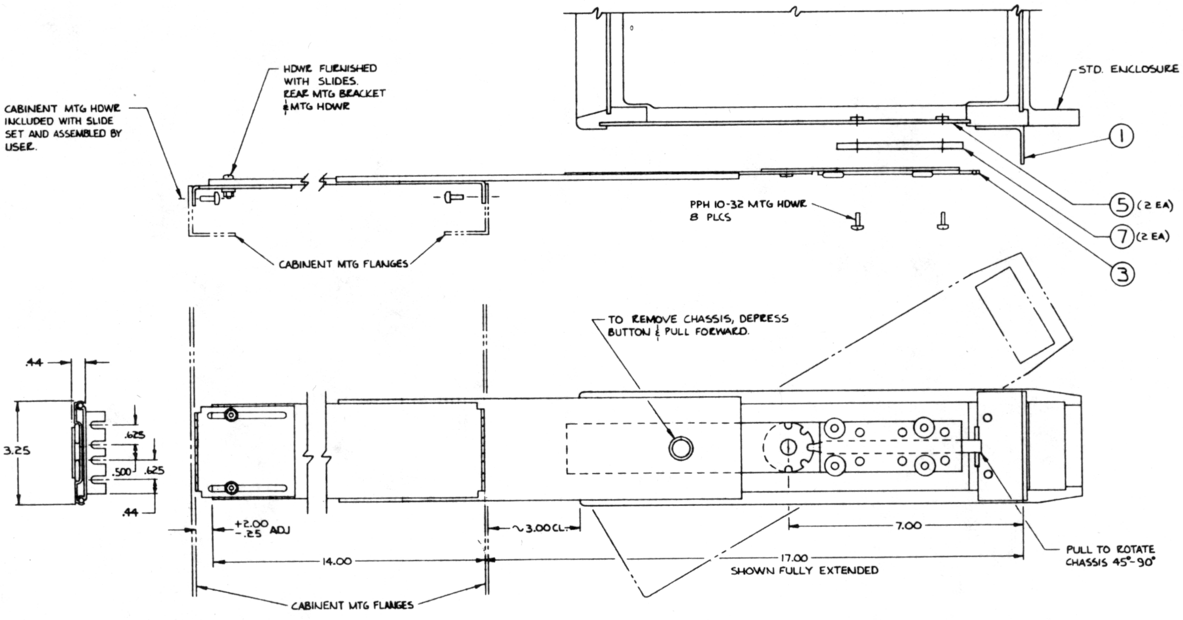
OPTION 10
CHASSIS SLIDE

Option 10 equips your counter with the hardware required to mount the unit in a standard 19" wide console. With the chassis slide installed the counter can be serviced without removing it from the rack.

The option consists of:

OPTION 10 – 2010147

① Rack Mount Kit – 2010008-01
③ Slide Set – 5000189
⑤ Side Panels – 5210179
⑦ Spacers – 5210249


HDWR FURNISHED WITH SLIDES. REAR MTG BRACKET & MTG HDWR
CABINENT MTG HDWR INCLUDED WITH SLIDE SET AND ASSEMBLED BY USER.
CABINENT MTG FLANGES
STD. ENCLOSURE
①
⑤(2 EA)
⑦(2 EA)
③
PPH 10-32 MTG HDWR 8 PLCS
TO REMOVE CHASSIS, DEPRESS BUTTON & PULL FORWARD.
.44
3.25
.625
.500
.625
.44
+2.00 -.25 ADJ
14.00
~3.00 CL.
7.00
17.00 SHOWN FULLY EXTENDED
PULL TO ROTATE CHASSIS 45°-90°
CABINENT MTG FLANGES

1. All MTG HDWR and hole spacing conforms to MIL-STD-189.
2. To install slides in field; Remove top cover and top frame; Mount special side panels (5210179) on Std. enclosure.
3. Item numbers within ○ symbol are on P/L 2010147. All other items assembled or exploded are shown for clarification or reference only.

Side View of Counter With Option 10 Installed

APPENDIX A
ACCESSORIES

MODEL 590 FREQUENCY EXTENSION CABLE KIT

The kit, part number 2000025 contains:

1 – LO Cable (long) – 2040217
1 – IF Cable (short) – 2040218
1 – Adaptor (SMA to TNC) – 2610063
0-4 – Remote Sensors (Options 91 thru 94)

REMOTE SENSOR OPTIONS

	PART NUMBER	FREQUENCY RANGE
91	2030022	26.5-40 GHz
92	2030029	40-60 GHz
93	2030030	60-90 GHz
94	2030031	90-110 GHz

SPECIFICATIONS

BAND 4
Used with 548A/06 Counter and 590 Frequency Extension kit

OPTIONS	91	92	93	94
SELECT BAND	**41**	**42**	**43**	**44**
Waveguide Band	Ka	U	E	W
Range	26.5-40 GHz	40-60 GHz	60-90 GHz	90-110 GHz
Sensitivity (typ)	-25 dBm (-20 dBm min.)	–25 dBm	–25 dBm	–25 dBm
Waveguide Size	WR-28	WR-19	WR-12	WR-10
Waveguide Flange	UG-599/U	UG-383/U	UG-387/U	UG-387/U
Max. Input (typ)	+5 dBm	+5 dBm	+5 dBm	+5 dBm
Damage Level	+10 dBm	+10 dBm	+10 dBm	+10 dBm

INSTALLATION

Before connecting the remote sensor to the frequency source, verify that the power level is within the limits specified for the sensor.

Connect the long LO cable from the upper jack to the remote sensor. When using the sensor option 91, use the SMA-TNC adaptor in the 590 kit.

Connect the short IF cable from the lower jack to the Band 3 input.

CAUTION

Static discharge or ground loops can damage or destroy the diode in a remote sensor. ALWAYS connect the LO cable to the counter first, then touch the shield to the body of the sensor before connecting.

Be sure that the counter and waveguide port, to which the sensor will connect have a common ground. If in doubt, connect with a ground strap before connecting the remote sensor.

OPERATION

After connection, select Band 41, 42, 43 or 44 on the 548A counter (equipped with option 06). Select the band by:

PRESS: [ ] [4] [1] or 42, 43 or 44.

Be certain that the band selected coincides with the remote sensor in use. See specifications Table.

NOTE

Frequency limits (low/high) and power meter function (Option 02) only operate to 26.5 GHz.

REPAIR

If loss of sensitivity occurs the diode in the sensor may be damaged. The 91 sensor diode can be replaced, all others require factory repair.

To replace the 91 sensor diode, unscrew the knurled cap and pull out the diode. Replace it with a 1N53B type diode that can be ordered from the manufacturer.

Alpha Industries, Inc.
20 Sylvan Road
Woburn, MA 01807

On order from EIP by part number 2730053.

EIP has an assembly exchange program for rapid repair of damaged units. Consult factory for details.